

# ADC performance in bench tests

BNL DUNE

David Adams

BNL

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# Introduction

I have been looking at ADC test data taken at BNL

- I report here on data taken in January 2017
  - ADC samples are read out for input voltage steps with sawtooth envelope
  - 20M samples for each ADC channel
    - approximately 4k samples for each ADC bin
  - Voltage offsets corrected February 2017
    - Some channels have 18M or fewer samples
- Data is from P1 chips
  - 35-ton used an earlier version
  - Expect this chip will be used for protoDUNE
- Data taken under different conditions
  - Warm (room temp) and cold (LN2)
  - Different sampling rates (1 and 2 MHz)
  - I have only looked at 2 MHz cold
  - All data taken with external clock

# Data taking

Data taken by the following team

- Hucheng Chen, Shanshan Gao, Jack Fried, Feng Liu (BNL)
- Damian Goeldi (Univ. of Bern)

Thanks to them to making this data available to me

Data format

- ADC samples
- Input voltage ramp from  $-300$  to  $1700$  mV in  $10$  s

Data taken for 25 ADC chips

- 16 channels each
  - I.e. a total of 400 ADC channels
  - And a total of 1.6M ADC bins (4096 bin/codes per channel)
- Chip placements:
  - Chip 0 is bare
  - Chips 2 and 4 are in board
  - Remainder are in a socket

# Voltage offset

## Input voltage is not measured directly

- For most samples, the saturated ADC response is used to infer the offset of the sawtooth input signal.
- For some channels, the ADC response dips back into range (i.e. not overflow) when the voltage is very high ( $> 1.7$  V)
  - This caused problems with the technique used to infer the voltage offset
  - Initial analysis showed some channels with 200 mV offsets
  - Calibration signal of 500 mV used to find the offsets for these channels
  - Chips 3, 6, 7, 17, 21, 22, 25, 26, 29, 32, 35 affected
    - Chip 6 is now broken and could not be calibrated
  - This “rollback” should not be a problem for DUNE because preamps saturate at 1.6 V
- Data given to me always has -300 mV for the first sample

# Response

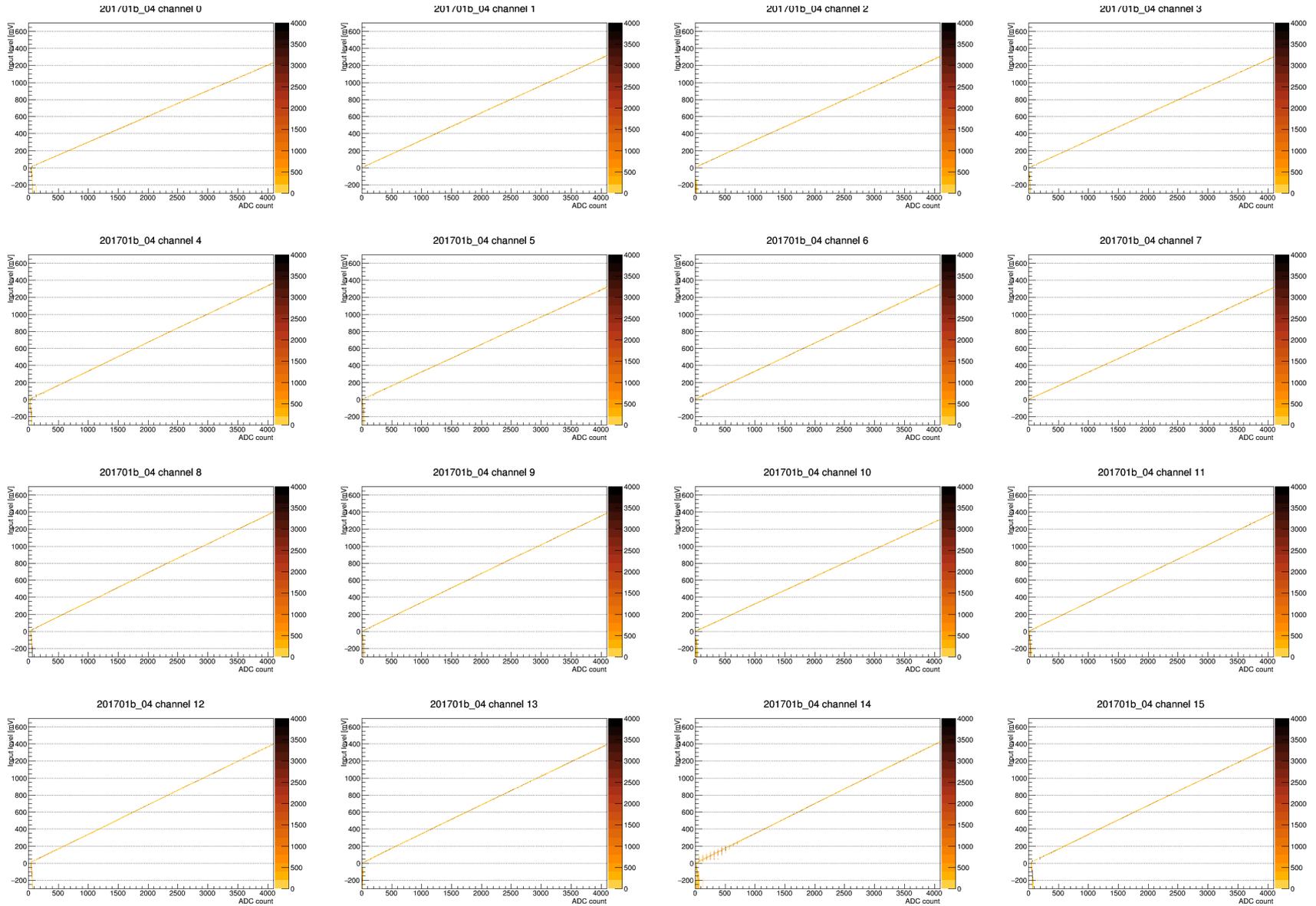
Following slides have response plots

- Input signal vs. ADC signal
- For chips 3 (good) and 7 (bad)
- No more 200 mV offsets
  - Except broken chip 6 which is still not calibrated correctly

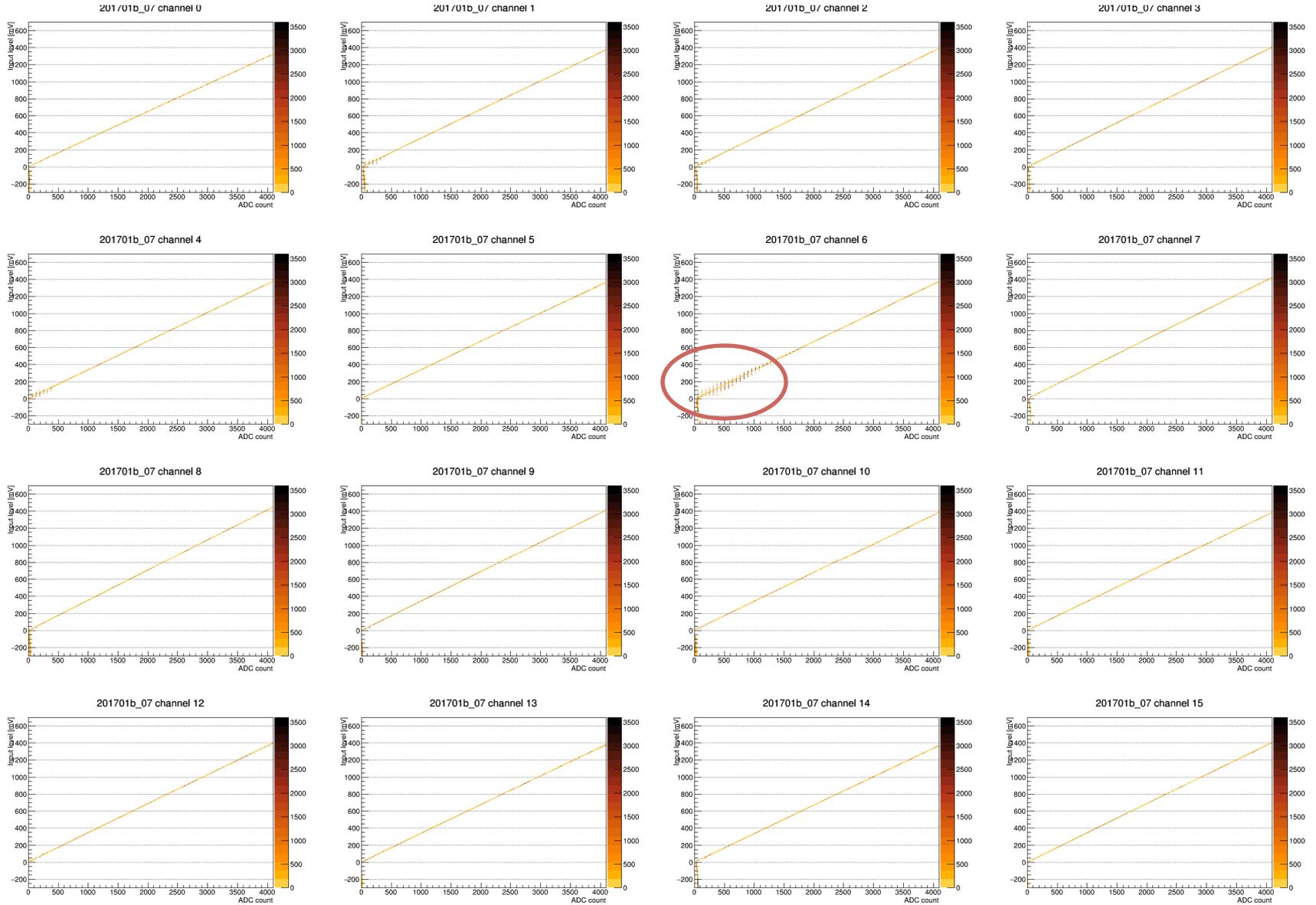
## Comments

- Plots look linear by eye (linear fit residuals in appendix)
- Often problems in lower ADC codes
  - Below 64 or 200 or 500+

# ADC chip 4 (good)



# ADC chip 7 (bad)



# Fits and residuals

## Linear fits

- I make a linear fit of the inverse response for each channel
  - $V_{in} = \text{gain} \times (\text{ADC code}) + \text{offset}$
  - Require  $64 < \text{ADC} < 4095$
  - And  $0 < V_{in} < 1600 \text{ mV}$
- Gain varies by  $\pm 5\%$  (RMS)
  - So we need a separate calibration for each channel
- Response show significant non-linearities
  - Evident in residual plots in appendix
  - Residual = difference between true and fitted  $V_{in}$
  - Plots show this residual for each ADC bin
- In addition, there are sticky bins
  - I.e. ADC codes for which a wide range of input voltages contribute
  - Vertical lines in the response and residual plots

# Fitted parameters

## Results of linear fits at right

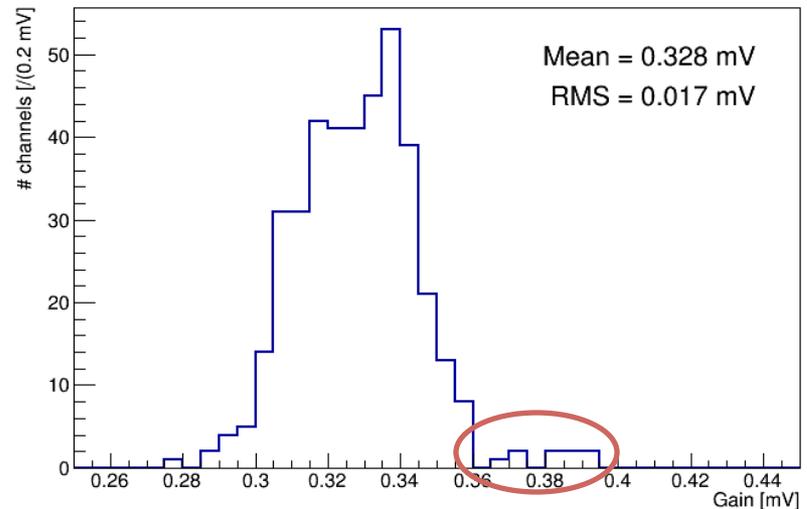
- Top is distribution of fitted gains
  - RMS is 5%
- Bottom is offsets

## Bad fits

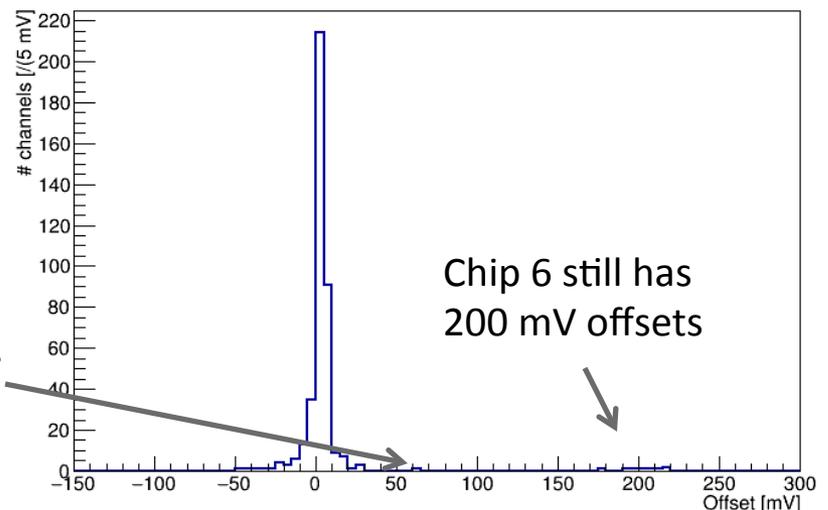
- There are bad fits for 18 of the 400 channels
- These give low offset and high gain (circled regions)
- See note following conclusions

Chip 22 channel 4 still has a large offset.  
It looks k=like ADC > 128 will fix this.

$V_{in}$ :ADC fit gain in mV/(ADC count)



$V_{in}$ :ADC fit offset



# Resolutions

We extract stats from the residual plots

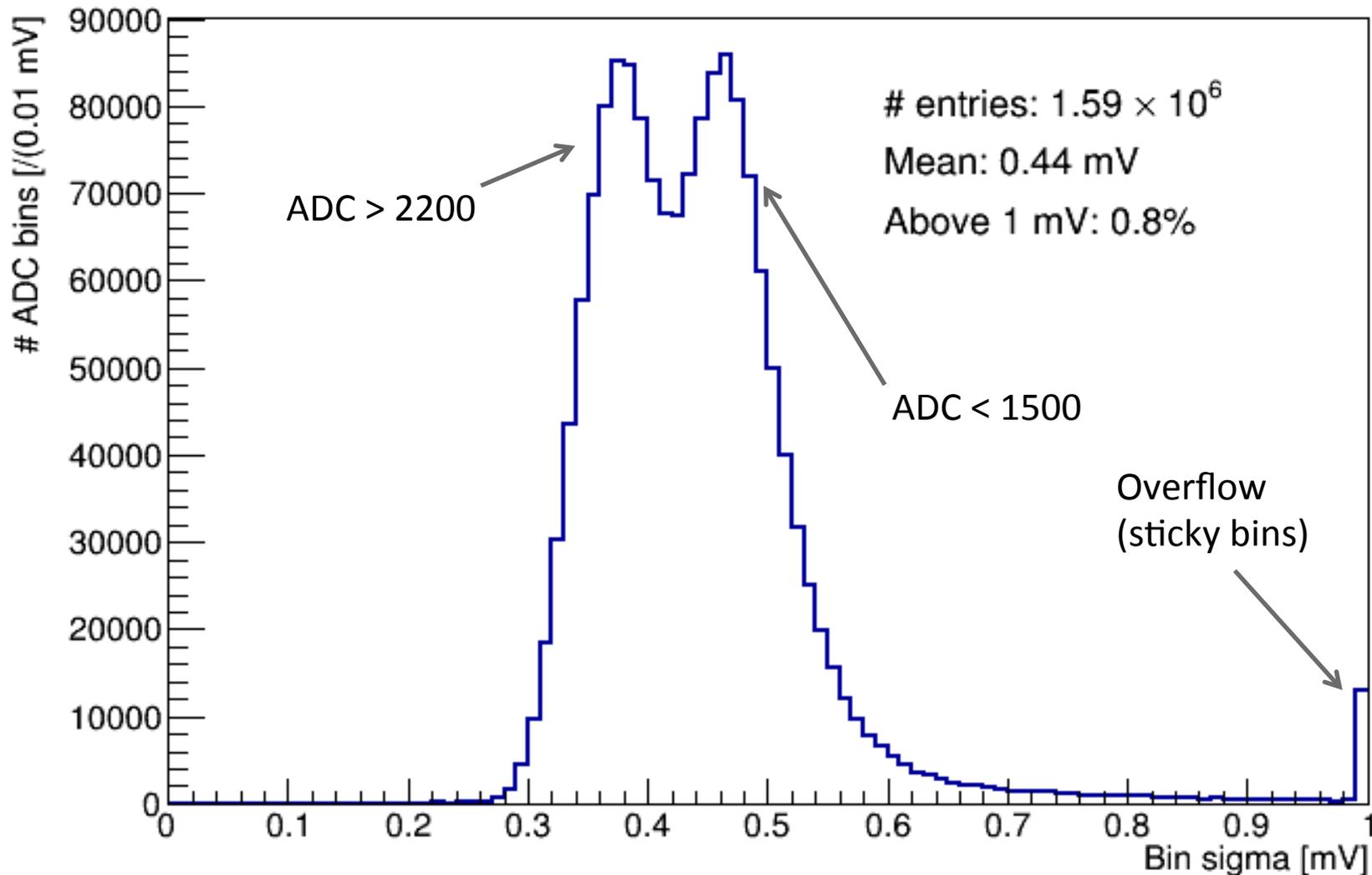
- Mean for each ADC bin
  - This is the “ultimate” calibration
- RMS of deviation from the mean
  - This is the resolution we get with ultimate calibration

Ultimate resolution

- I.e. that obtained with the ultimate calibration
- Varies from bin to bin
- Large for sticky bins
- Distribution for all bins on following slide

# Ultimate resolution

ADC bin resolution ( $65 < \text{ADC} < 4095$ )



# Metrics

Want to develop metrics to characterize ADC quality

- So we can decide which chips to use in protoDUNE
- Plan to produce 3000 chips and select 1000 for the detector

Voltage range covered by the chip

- May be different for each channel on a chip
  - Some have 200 mV offset and some don't
- I use the the endpoints of linear calibration to evaluate this range
  - ADC bin 65 for the low end because lower bins are often bad
  - ADC bin 4094 for the high end (4095 is overflow)
- Shown as points on the metric plot

Fraction of bins with bad resolution (i.e. that are sticky)

- Define bad with a cut on the (ultimate) resolution
- Note that 1.0 mV corresponds to
  - $(6240 \text{ e/fC}) / (14 \text{ mV/fC}) = 450 \text{ e}$

# Metrics (cont.)

## Efficiency

- Preceding are useful but only give the performance of each ADC bin
- Want to know what fraction of input signals appear in good bins
- Define efficiency to be the fraction of input signals that fall in bins below some  $\text{RMS}(V_{\text{in}})$  threshold
  - Here use  $\text{RMS} < 1.0 \text{ mV}$
- Evaluate efficiency in bins of input voltage
  - Plots for all channels in appendix (also include resolution)
  - Following page has summary for all channels.

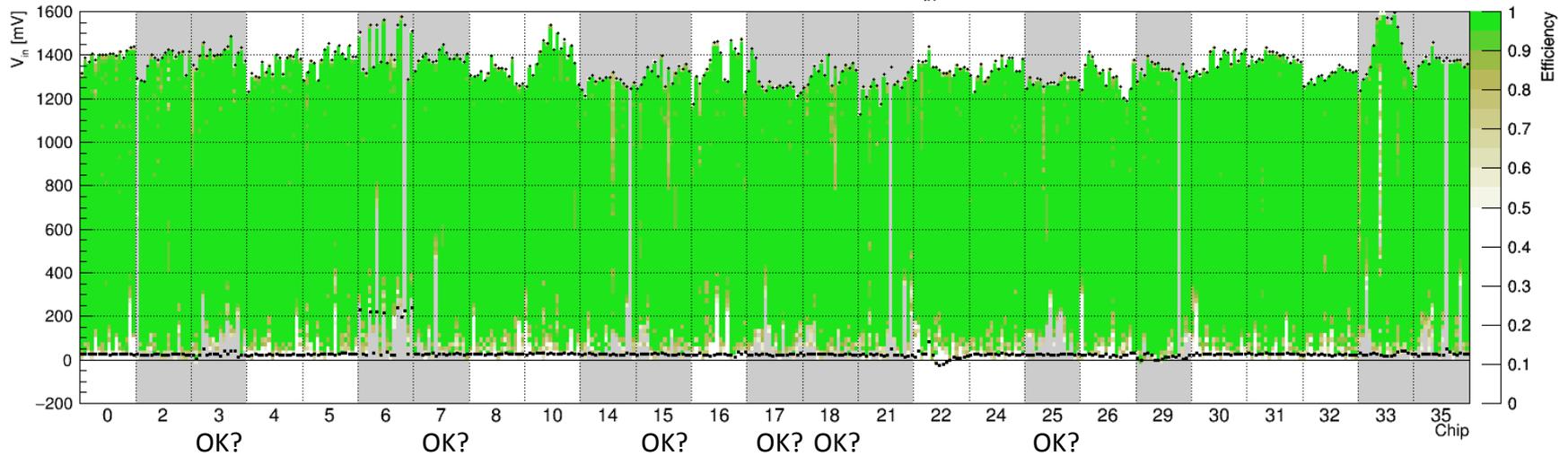
## Better channels are shown with white BG

- I selected 12 chips to get the desired yield
  - Require all channels for each to be “good”
  - About 1/2 of the studied sample (25 chips)
  - About 1/3 of the 35 fabricated
    - Remaining 10 could not be used
    - Possible to recover some of these with extra effort?

# Metrics: Summary plots

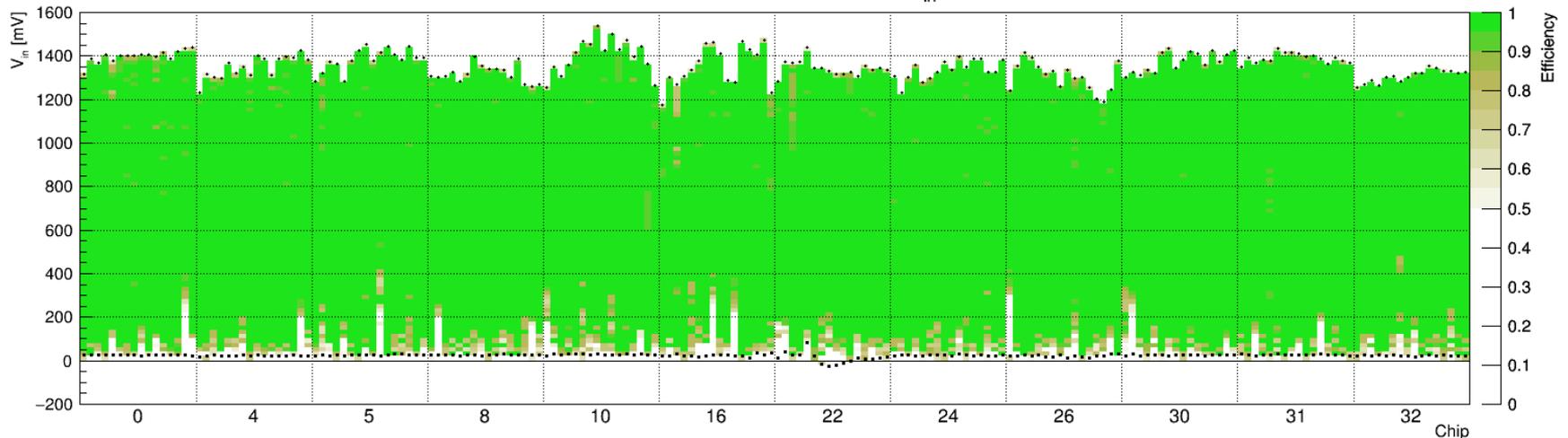
Input voltage efficiency for  $\text{RMS}(V_{in}) < 1 \text{ mV}$

All chips



Input voltage efficiency for  $\text{RMS}(V_{in}) < 1 \text{ mV}$

Selected chips

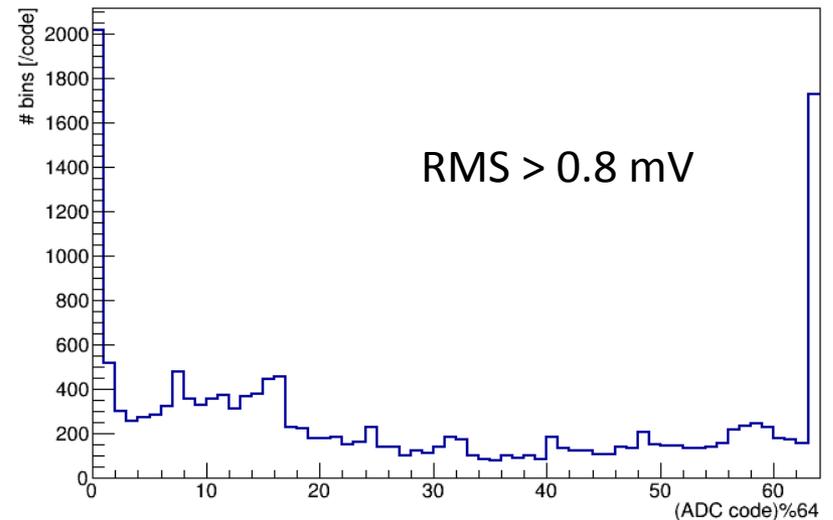


# Sticky codes

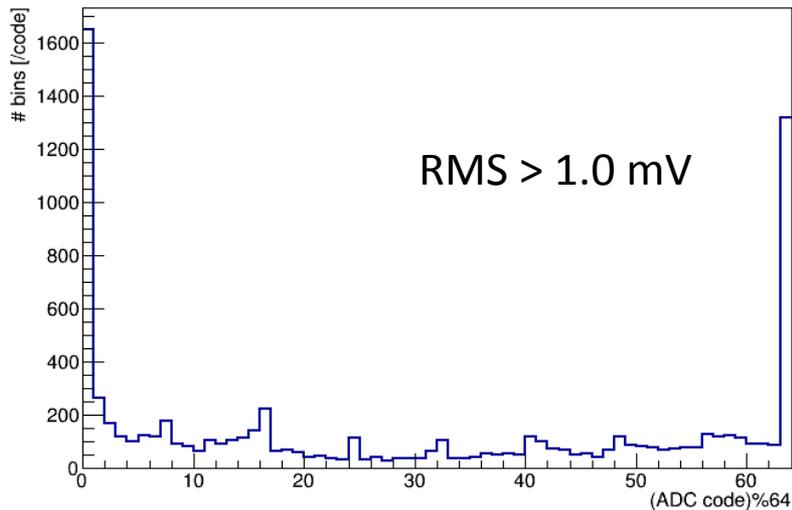
## Which codes are sticky?

- Plots at show the the 6 LSB (least significant bits) for the bad bins
  - For 3 RMS( $V_{in}$ ) thresholds
- Most often but not always the classic values of 0 and 63

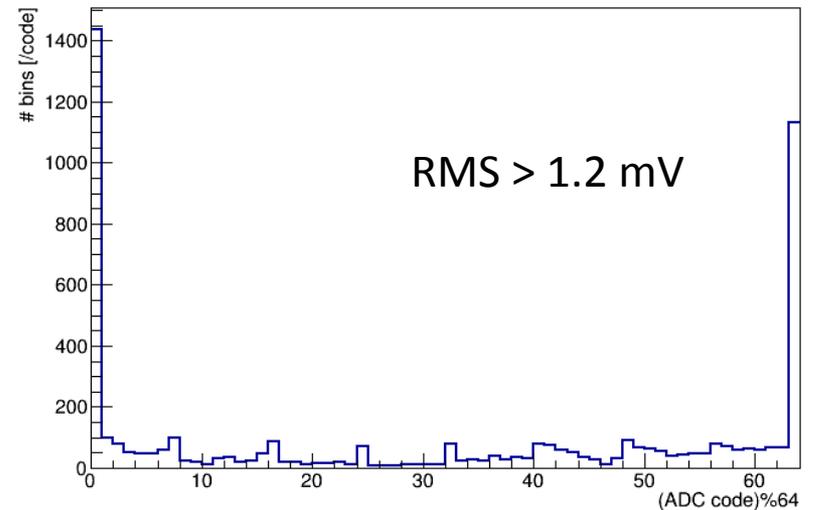
ADC bad code distribution (512 < ADC < 4095, RMS > 0.8 mV)



ADC bad code distribution (512 < ADC < 4095, RMS > 1 mV)



ADC bad code distribution (512 < ADC < 4095, RMS > 1.2 mV)



# Comments and conclusions

## ADC response

- ADCs show non-negligible nonlinearities
  - We will want many-parameter calibration for each channel
  - 4000 parameters (one/bin) for ultimate calibration
- In addition there are bins that cannot be used
  - Populated by a wide range of input voltages (sticky)
  - Identified by poor “ultimate” resolution
- Resolution is typically 0.5 mV (230 e) for the good bins

## Chip selection

- We plan to use/fabricate 1000/3000 chips
- Many chips have problems with one or two channels
- Propose to use efficiency as function of  $V_{in}$  to rank chips
  - Efficiency is fraction of samples with  $RMS(V_{in})$  below some threshold
    - Here 1.0 mV (450 e)
- Try to find chips where all channels are “good”
  - Settle for one or two “fair” channels

# Comments and conclusions (2)

## Selection results

- I selected 12 of the 35 fabricated chips to get the desired yield
- Useful input voltage range is (200, 1200) mV for most channels
  - Few channels only become useful at 300 mV
  - Many extend up to 1300 or 1400 mV and/or down to 100 mV
  - Preamp output is (0, 1600 mV)
- Need to set a pedestals to capture signals below zero
  - 500 mv for collection planes
    - Want pedestal (and signal) to be in region of high efficiency
  - 700 mV for induction
    - Same range for each sign

## Future studies

- Correlations in time (tick-to-tick)
- Change in response and bad channels with time (week, month, ...)

# Update Feb 27

## Problem found in analysis on which these results are based

- Linear fit was poor for 18 of the 400 channels used here
- Apparently because  $V_{in} < 0$  populates ADC bins above 64 for these channels
  - Fit range was (64, 4095)
  - I added requirement that  $V_{in}$  is in (0, 1600) mV
- Now see some changes:
  - Gain and offset distributions (see note added on that page)
  - The linear-fit voltage ranges (black points) on the metric summary plot
  - Distribution for linear calibration resolution tail reduced

# Appendix

Resolution distribution for linear calibration

Effective # bits

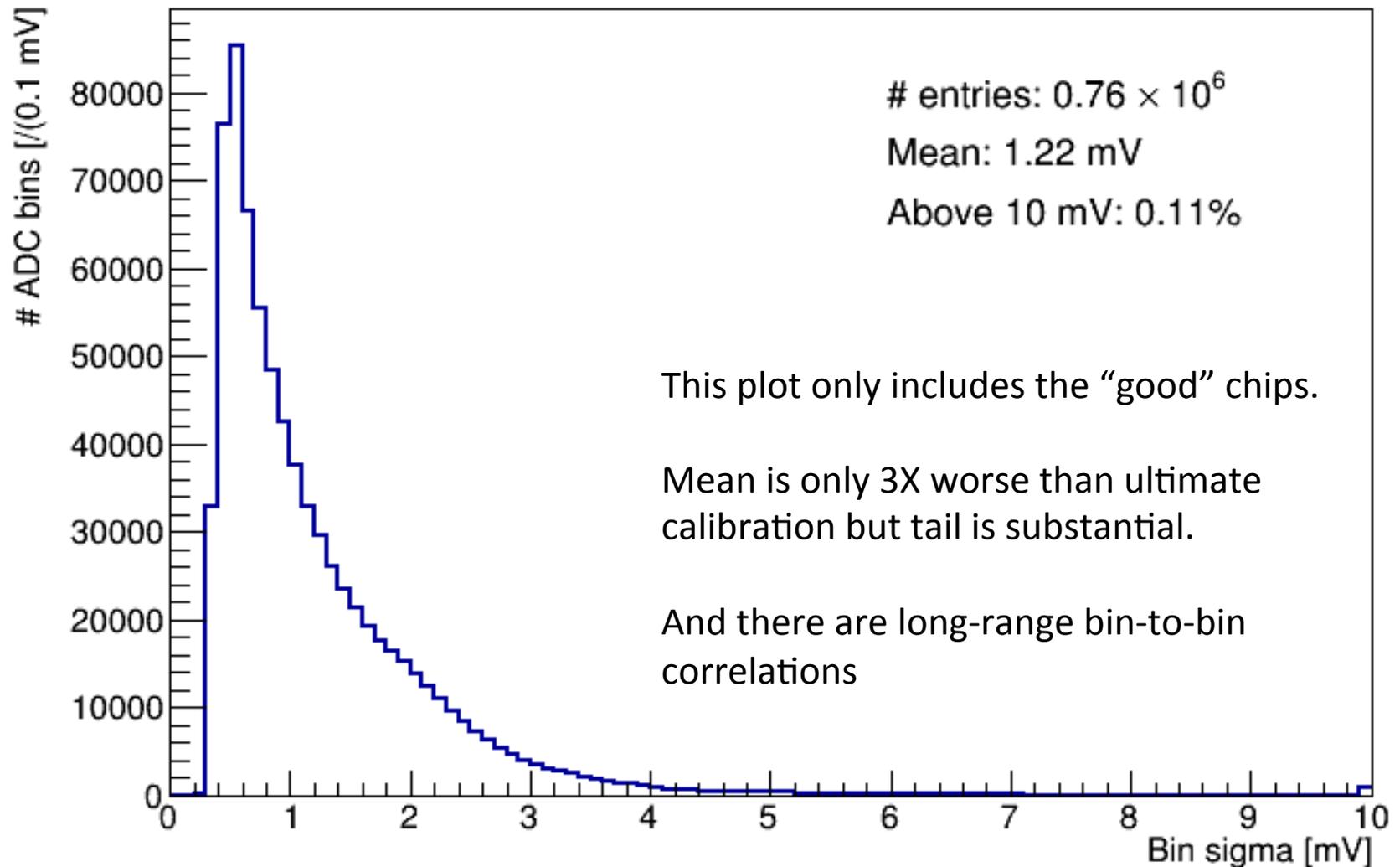
Voltage response for example bad bins

Residual plots for all chips

Efficiency vs.  $V_{in}$  for all chips

# Resolution distribution for linear calibration

ADC bin resolution ( $65 < \text{ADC} < 4095$ , good) for linear calib



# Effective number of bits

Sometimes useful to characterize ADC with effective # bits,  $N_e$ :

$$\sigma_V = \sigma_0 2^{(12-N_e)}$$

where  $\sigma_V$  is the measured resolution (on the input voltage)

and  $\sigma_0$  is the ideal resolution:

$$\sigma_0 = g/\text{sqrt}(12) = (0.328 \text{ mV})/\text{sqrt}(12) = 0.095 \text{ mV}$$

using the average gain for the ADCs analyzed here.

The effective # bits is then

$$N_e = 12 - \log(\sigma_V/\sigma_0)/\log(2)$$

Table shows effective # bits

- For various resolutions
- The effective # bits for the good bins here are 9-10

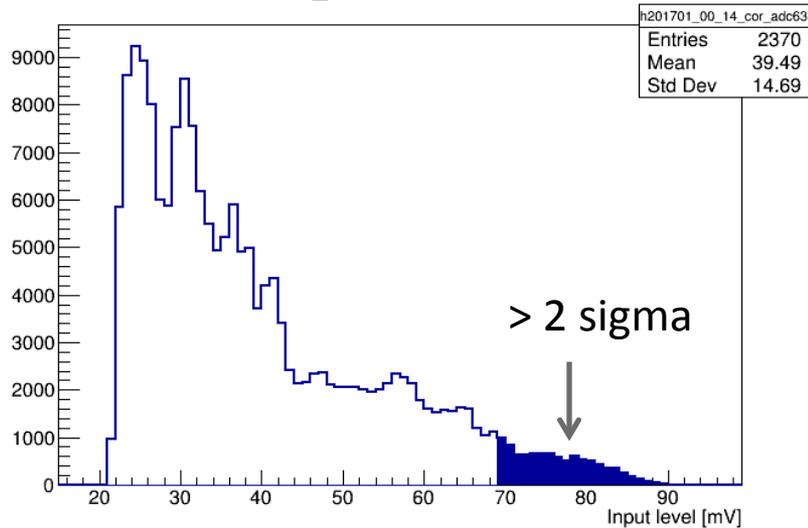
N	$\sigma_V$ (mV)
12	0.095
11	0.19
10	0.38
9	0.76
8	1.5
7	3.0
6	6.1



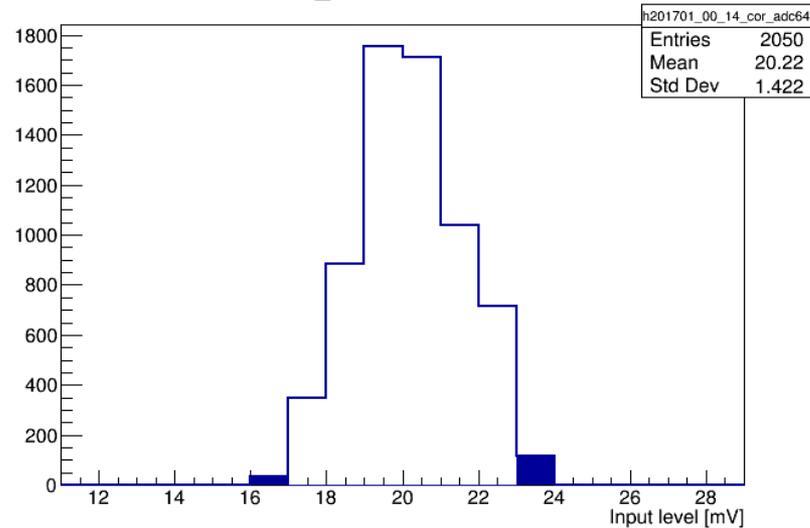
## Voltage response for example bad bins

# Chip 0 channel 14

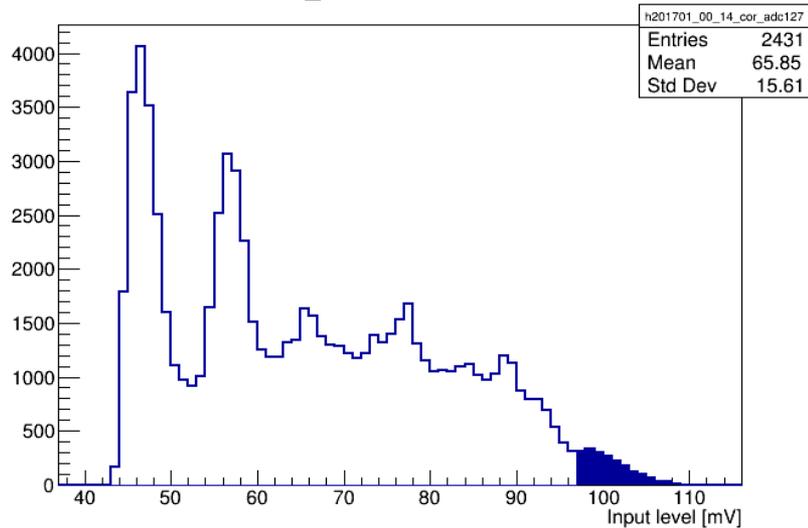
201701\_00 channel 14 bin 63



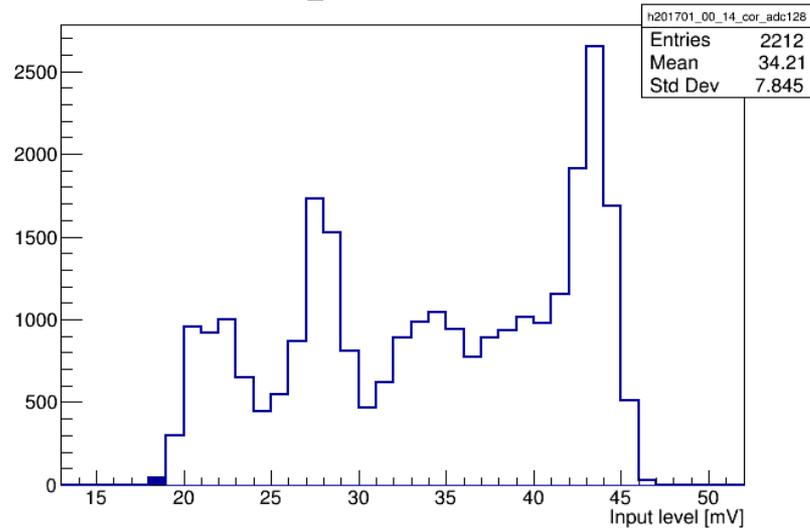
201701\_00 channel 14 bin 64



201701\_00 channel 14 bin 127

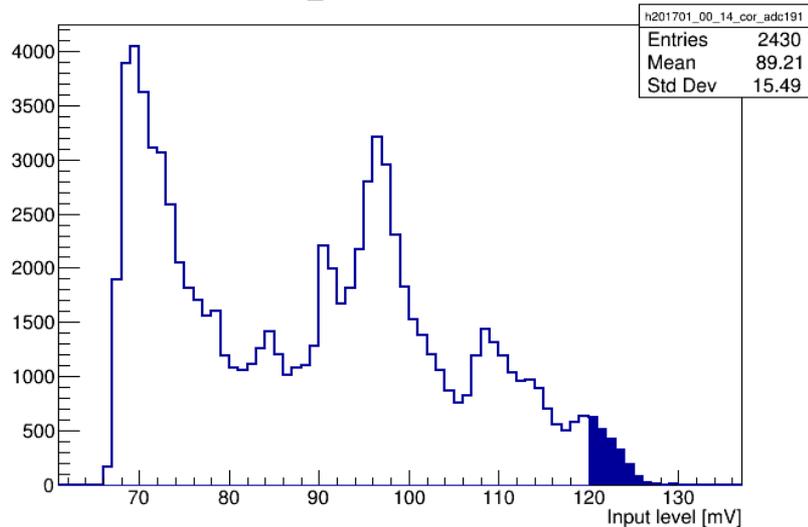


201701\_00 channel 14 bin 128

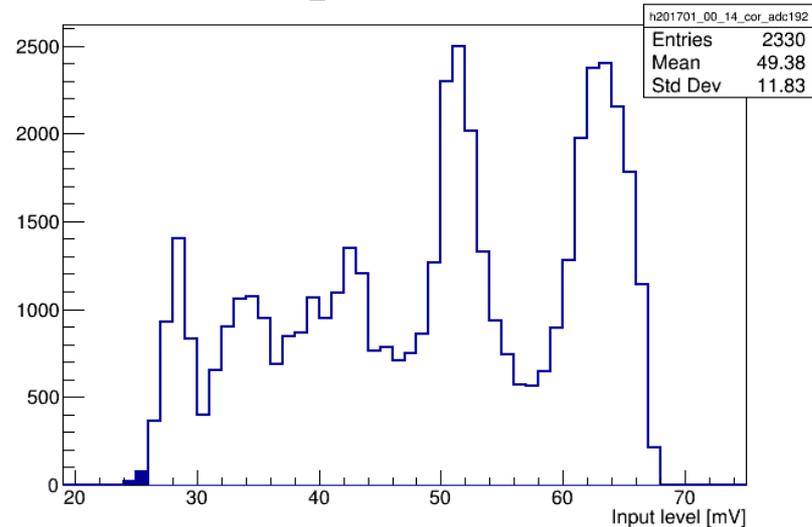


# Chip 0 channel 14

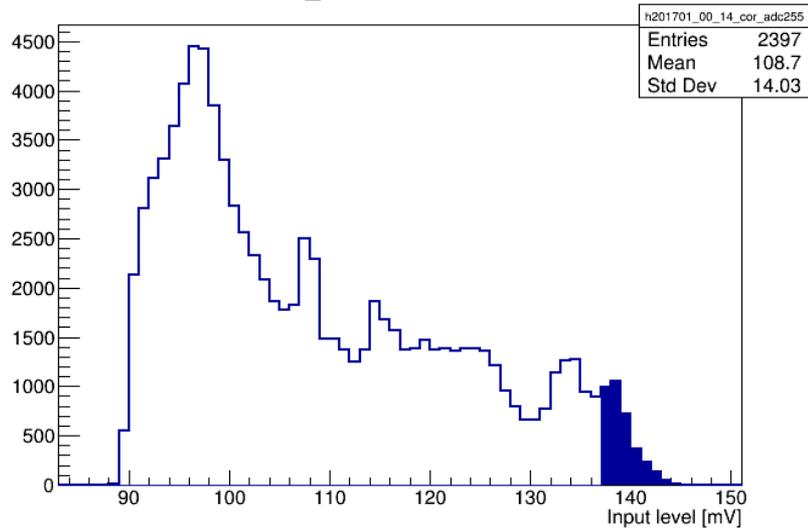
201701\_00 channel 14 bin 191



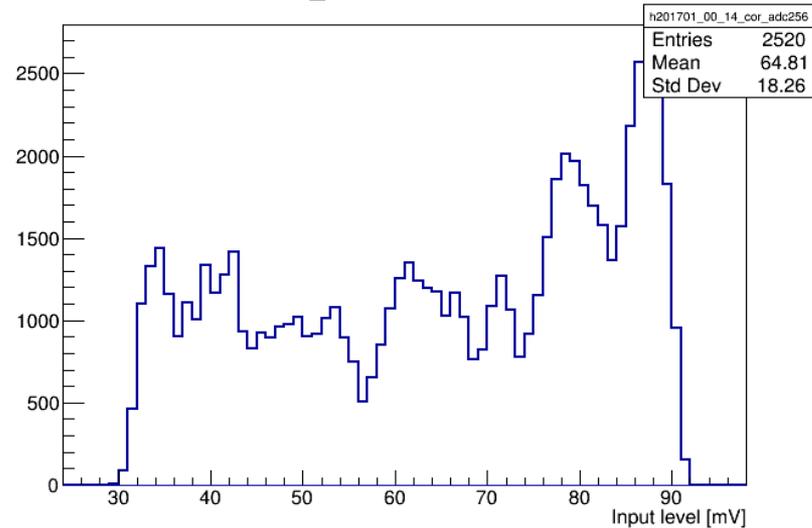
201701\_00 channel 14 bin 192



201701\_00 channel 14 bin 255

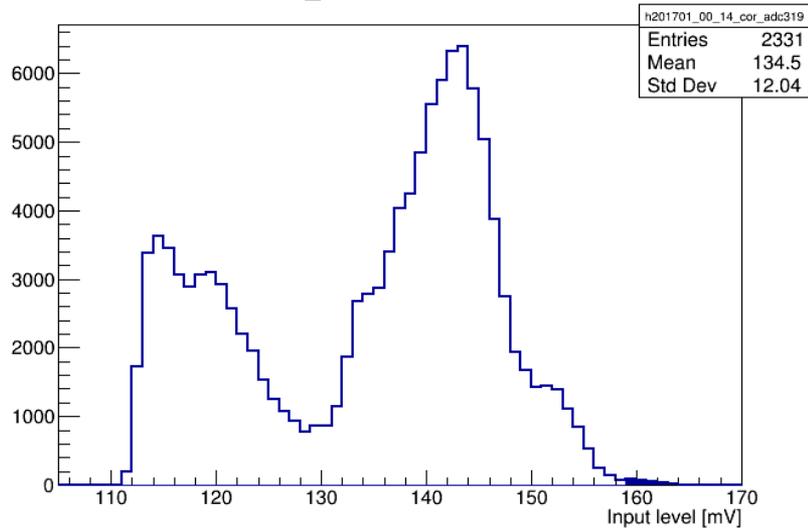


201701\_00 channel 14 bin 256

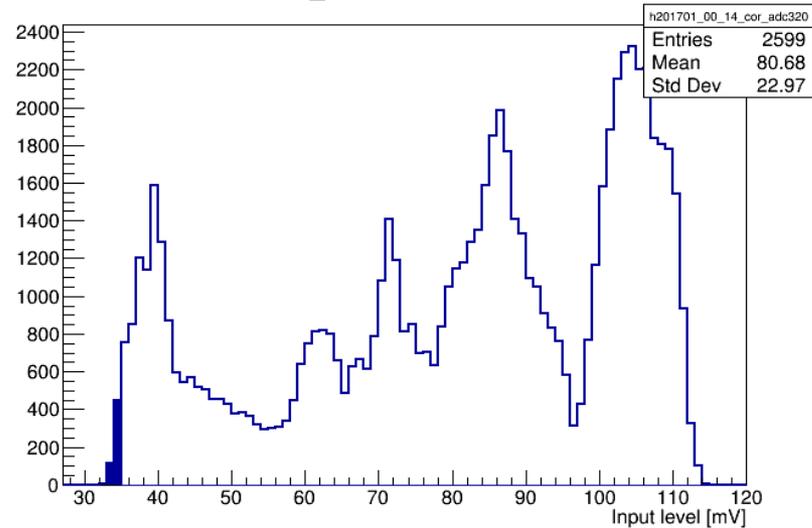


# Chip 0 channel 14

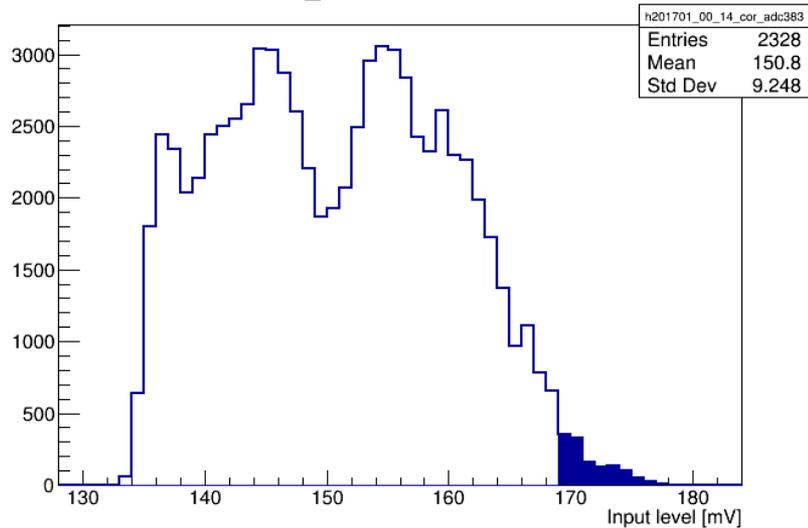
201701\_00 channel 14 bin 319



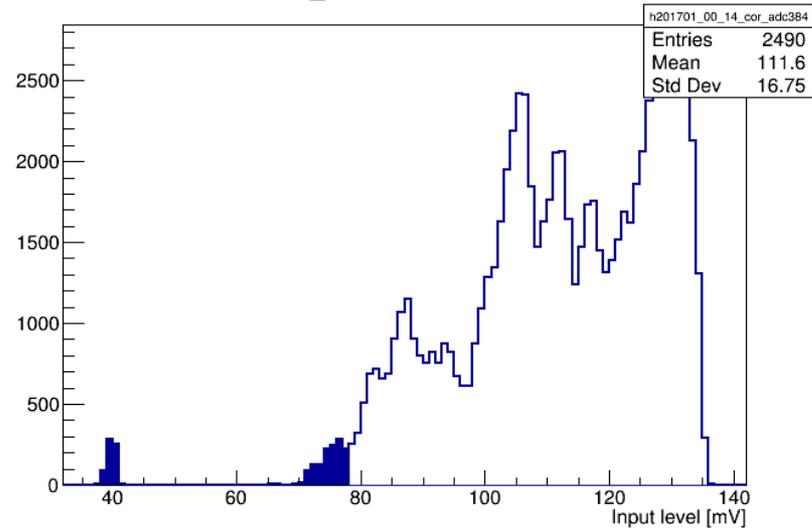
201701\_00 channel 14 bin 320



201701\_00 channel 14 bin 383

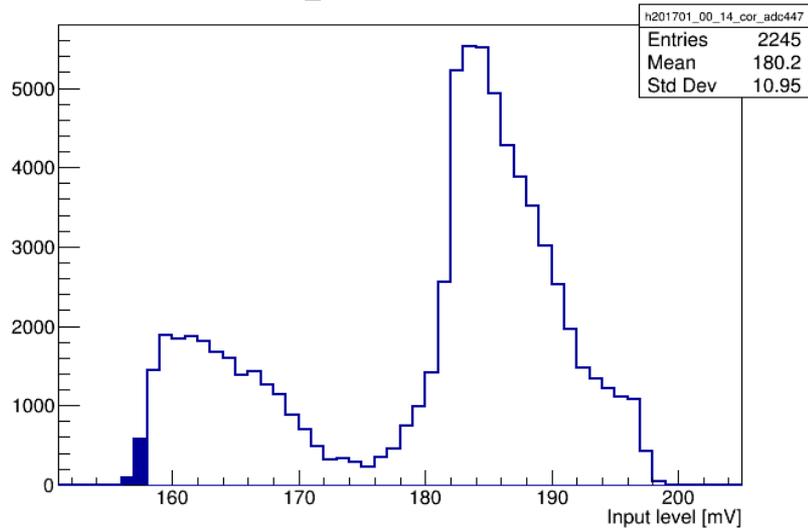


201701\_00 channel 14 bin 384

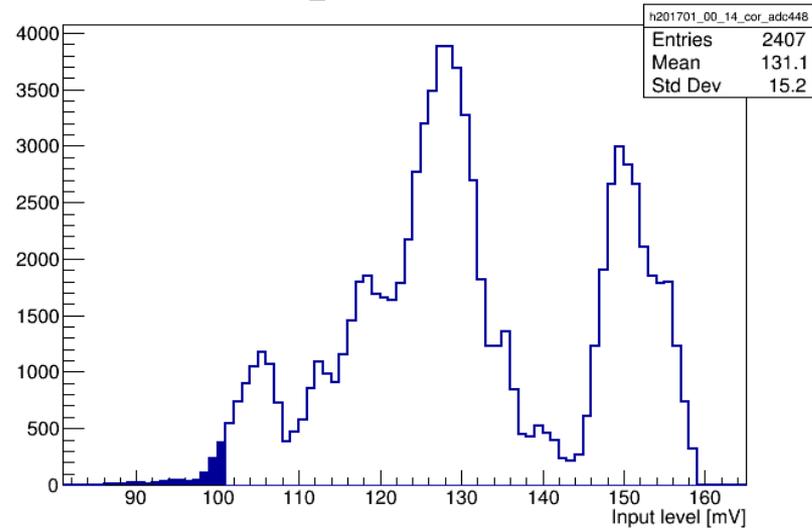


# Chip 0 channel 14

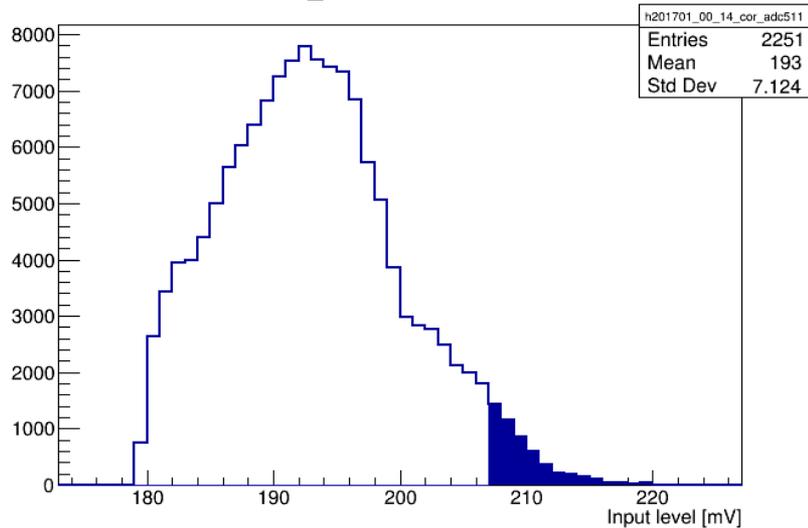
201701\_00 channel 14 bin 447



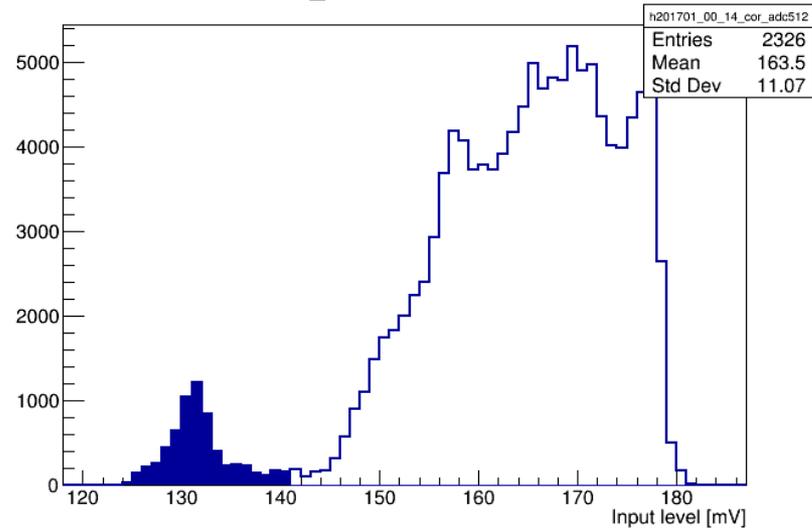
201701\_00 channel 14 bin 448



201701\_00 channel 14 bin 511

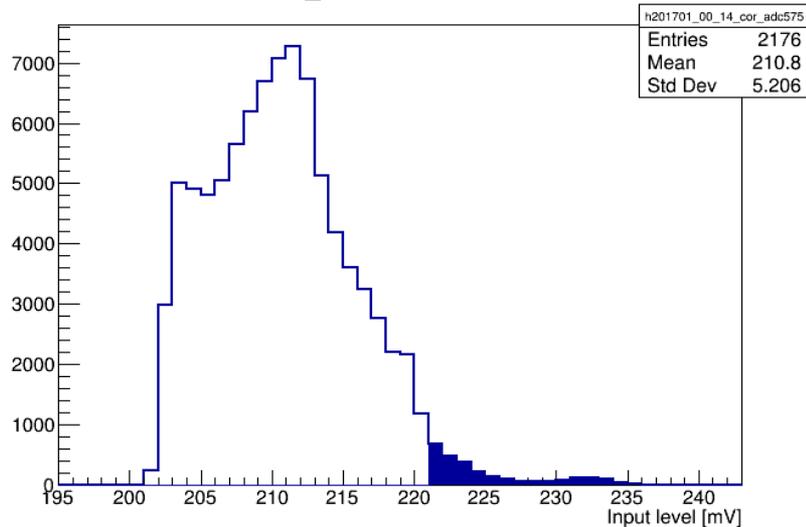


201701\_00 channel 14 bin 512

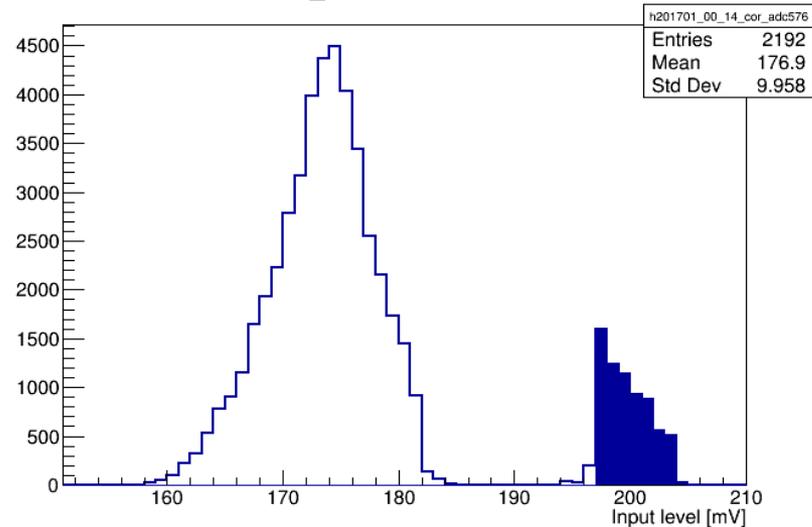


# Chip 0 channel 14

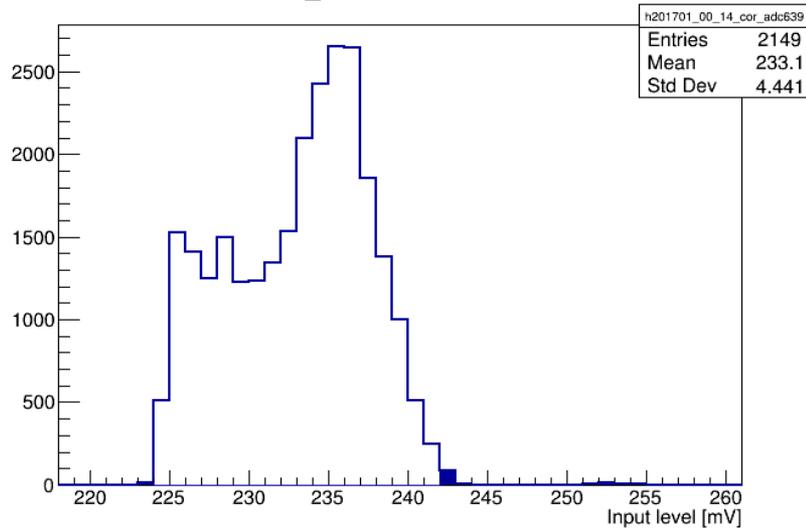
201701\_00 channel 14 bin 575



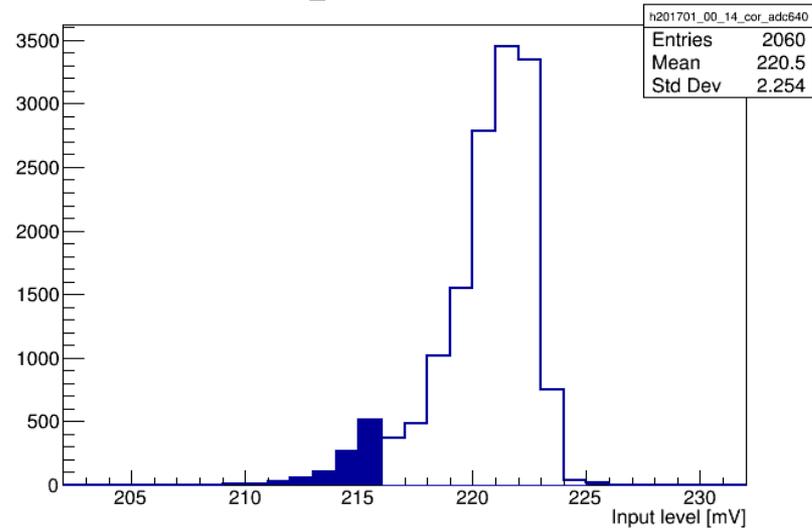
201701\_00 channel 14 bin 576



201701\_00 channel 14 bin 639

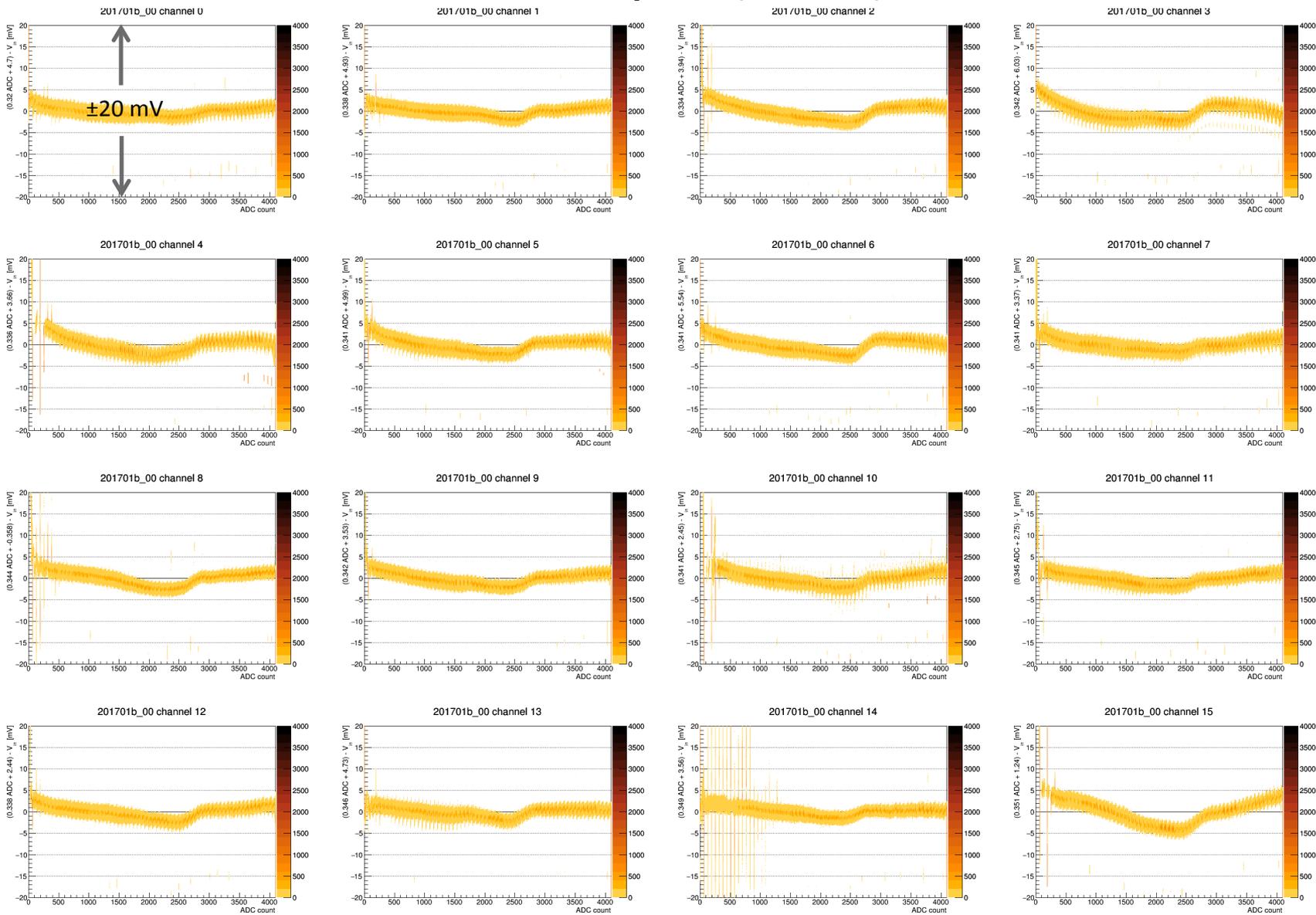


201701\_00 channel 14 bin 640

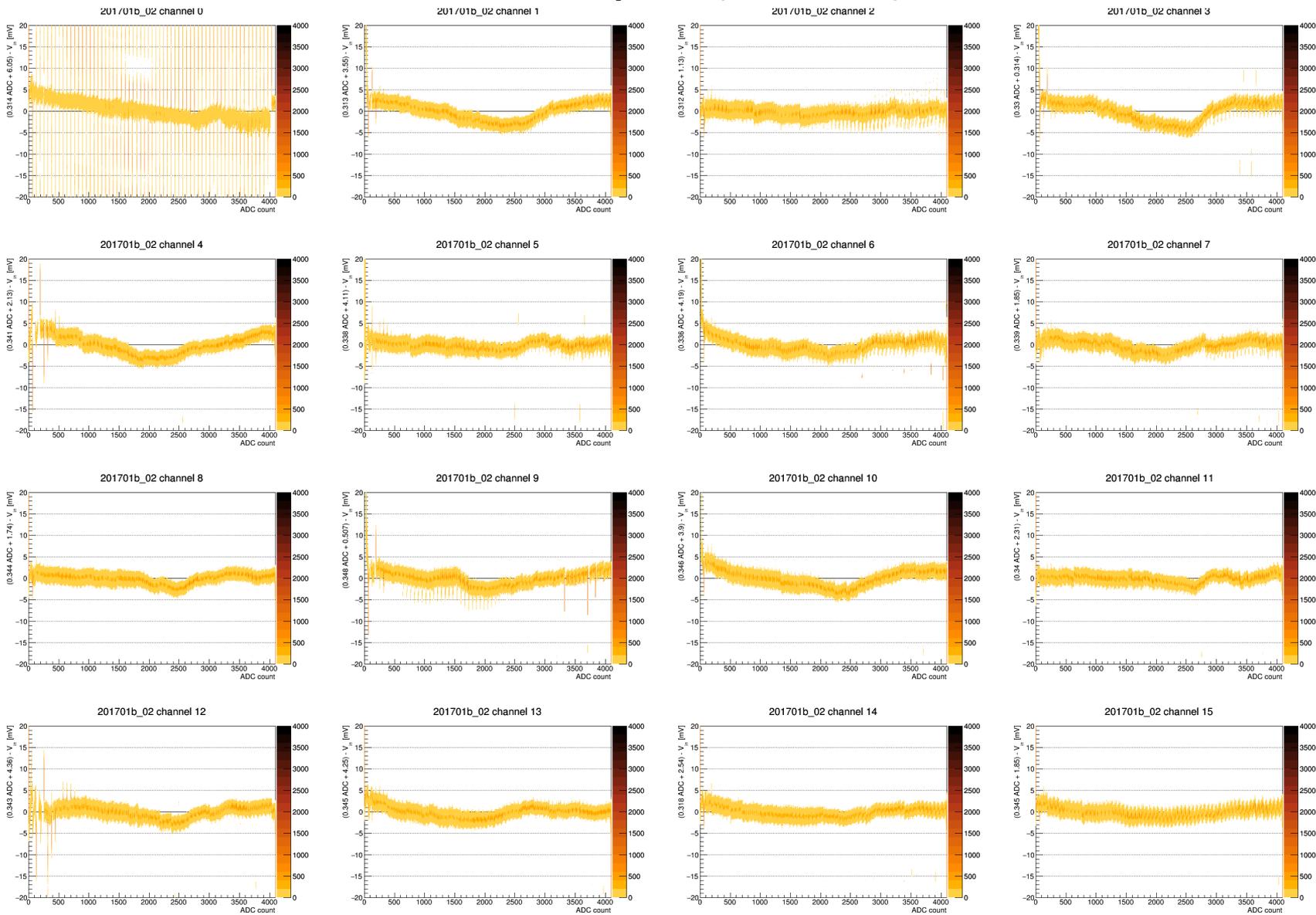


# Residual plots for all bins

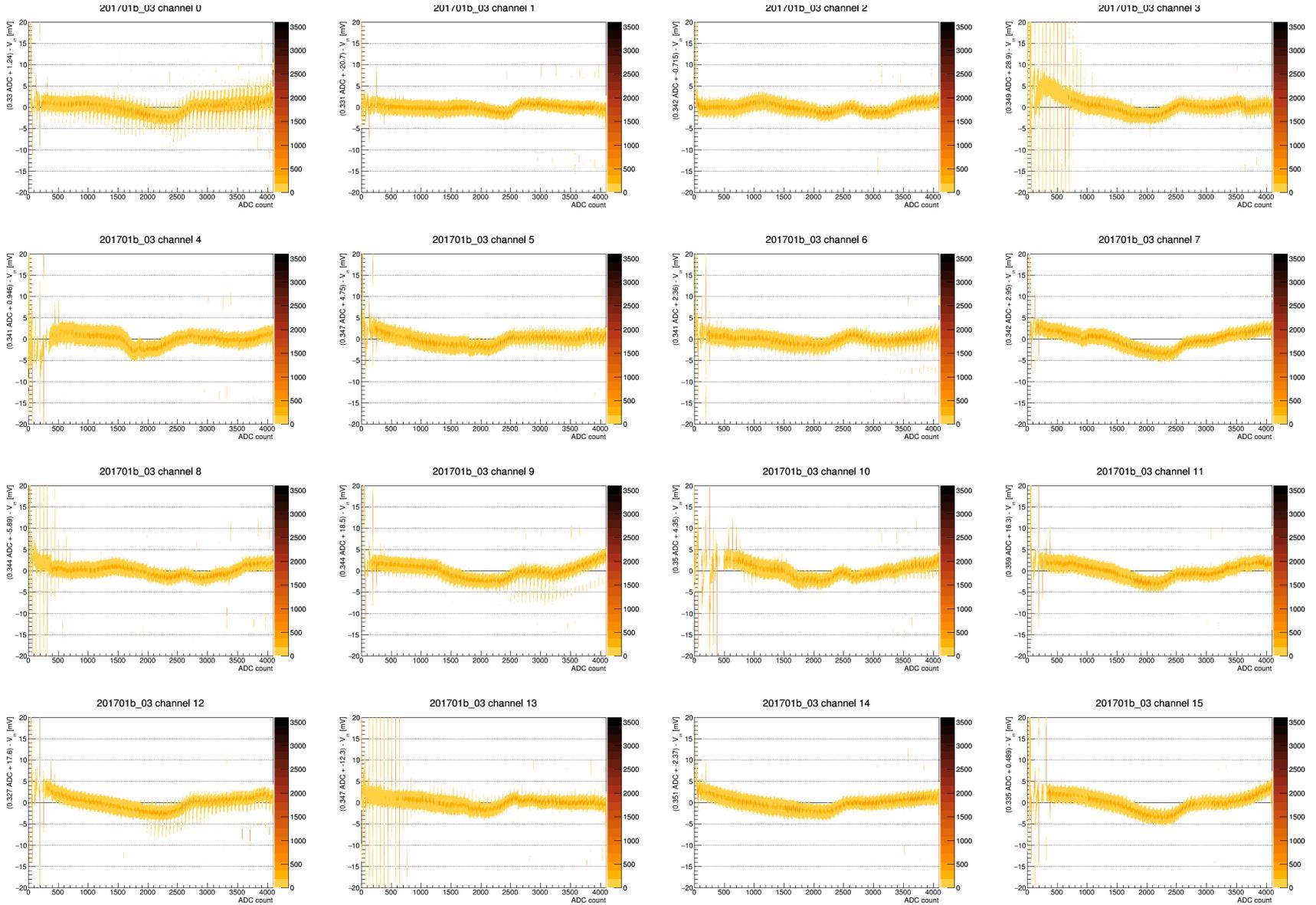
# ADC chip 0 (bare)



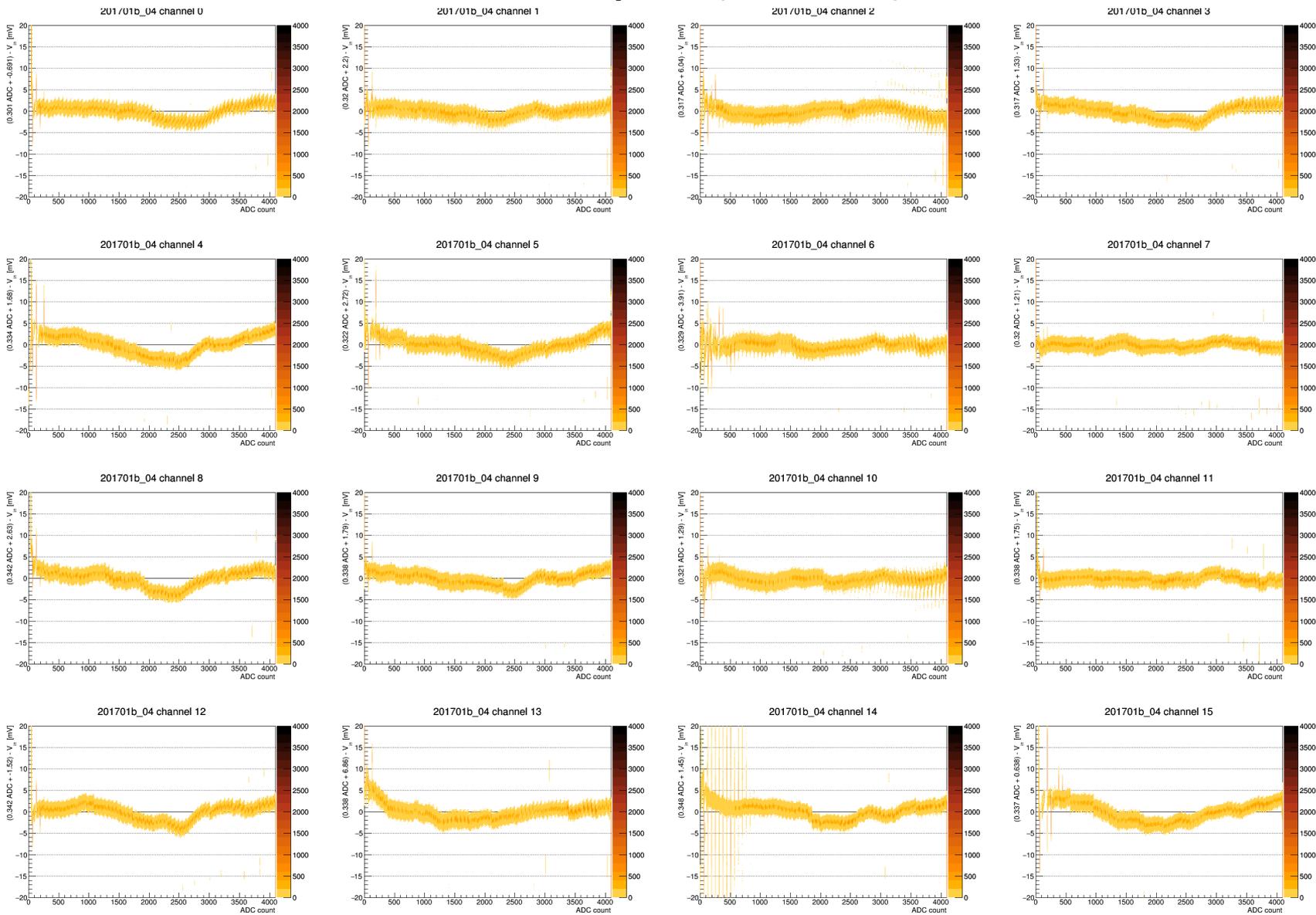
# ADC chip 2 (board)



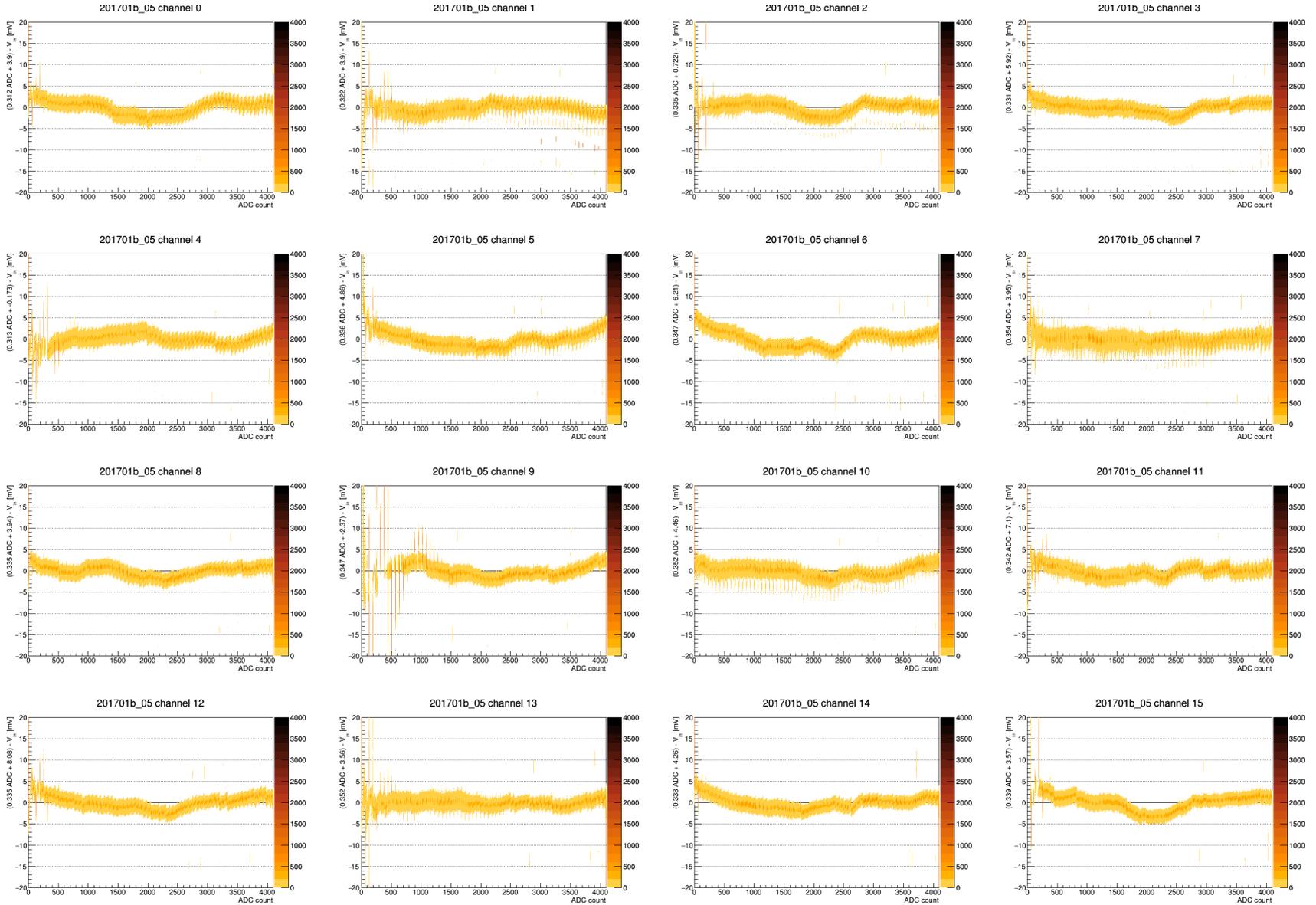
# ADC chip 3



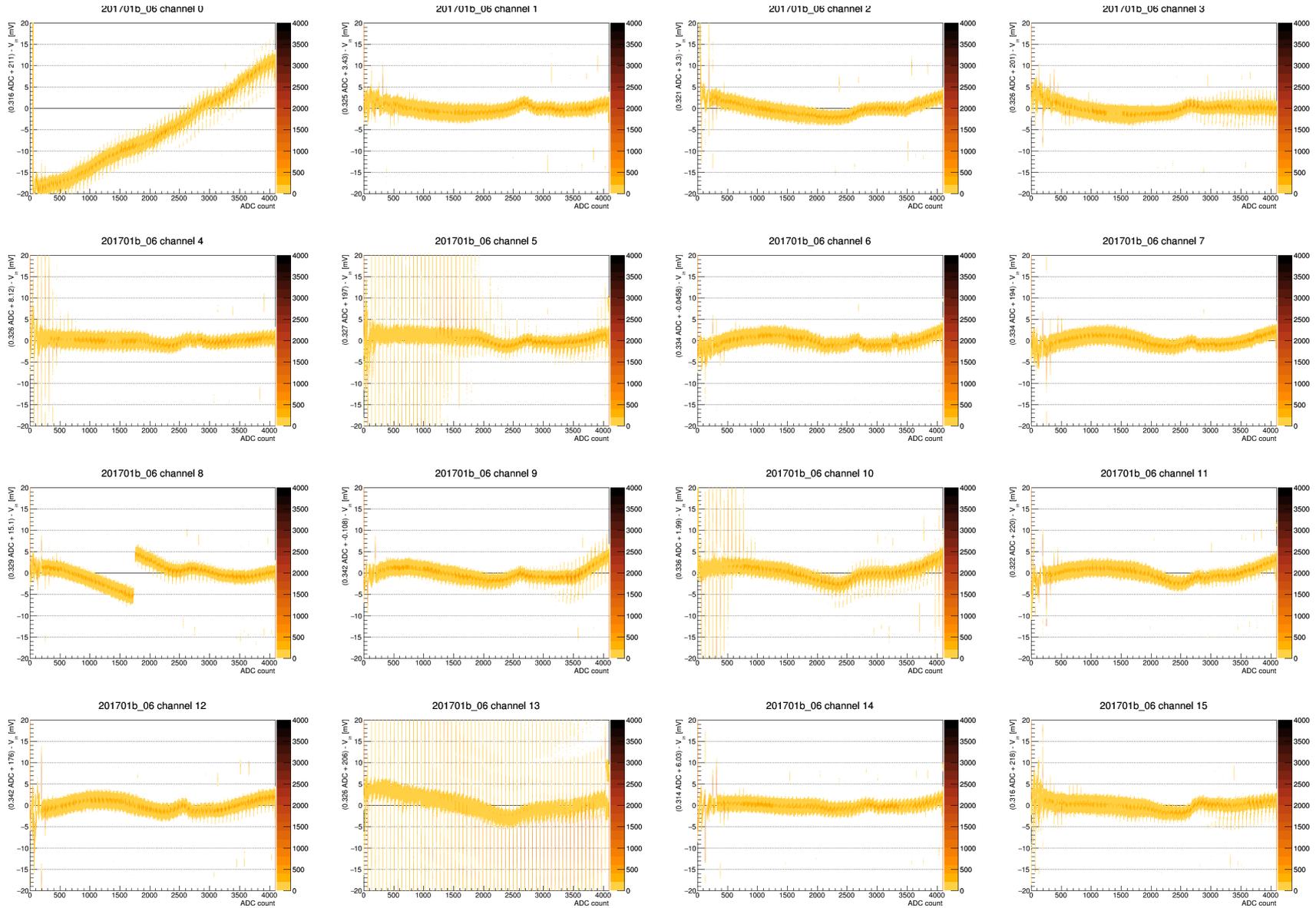
# ADC chip 4 (board)



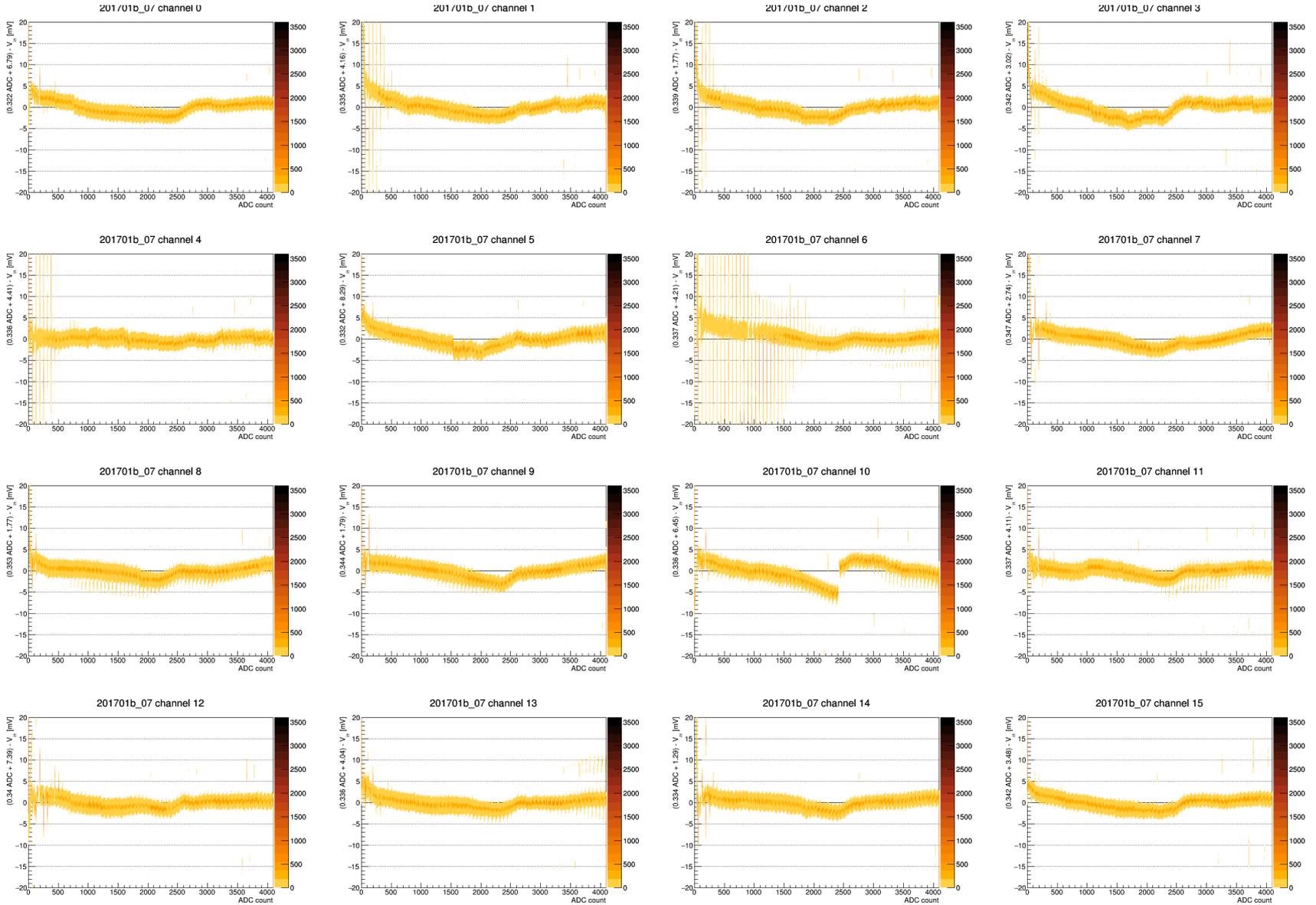
# ADC chip 5



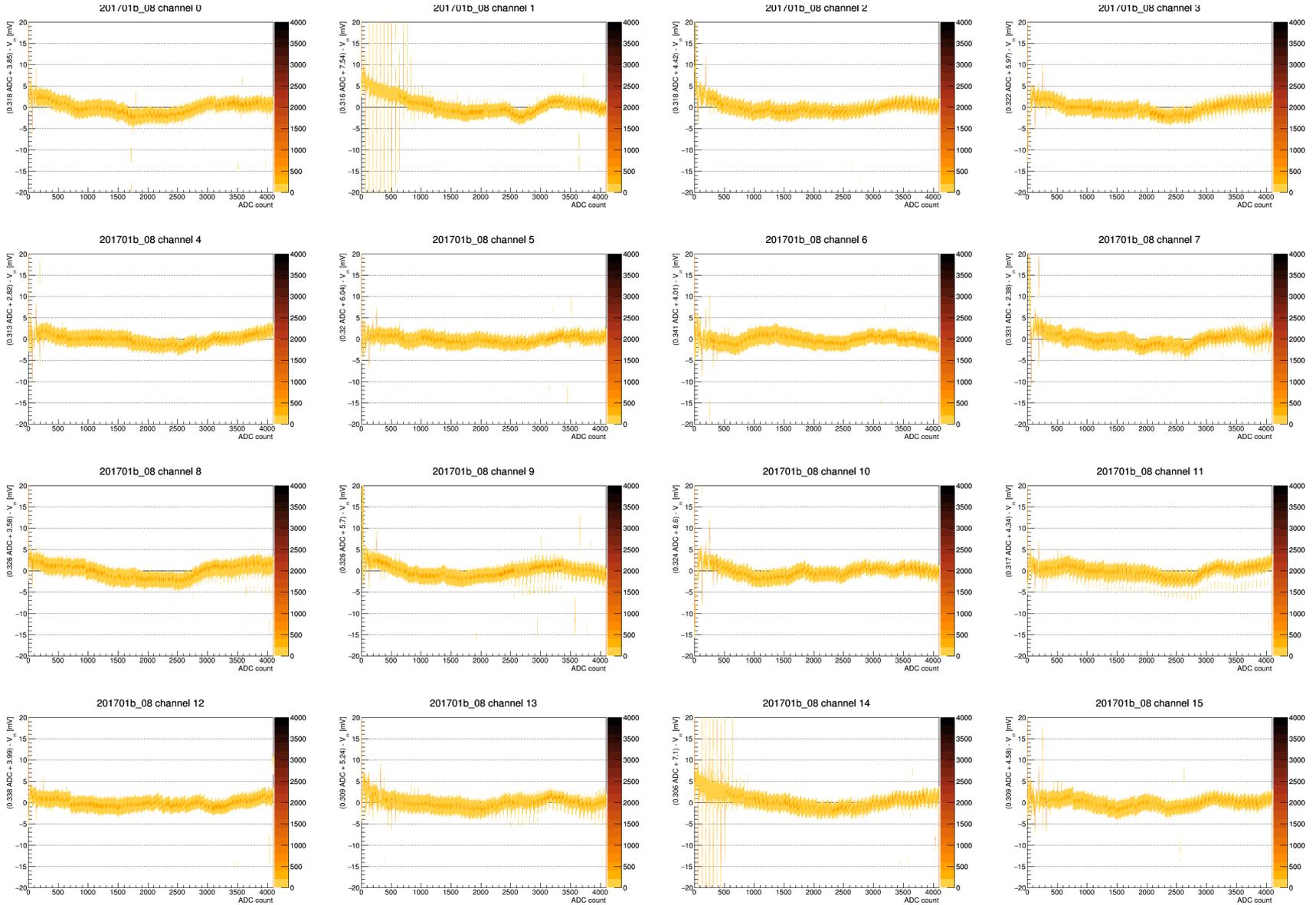
# ADC chip 6 (voltage offset not corrected)



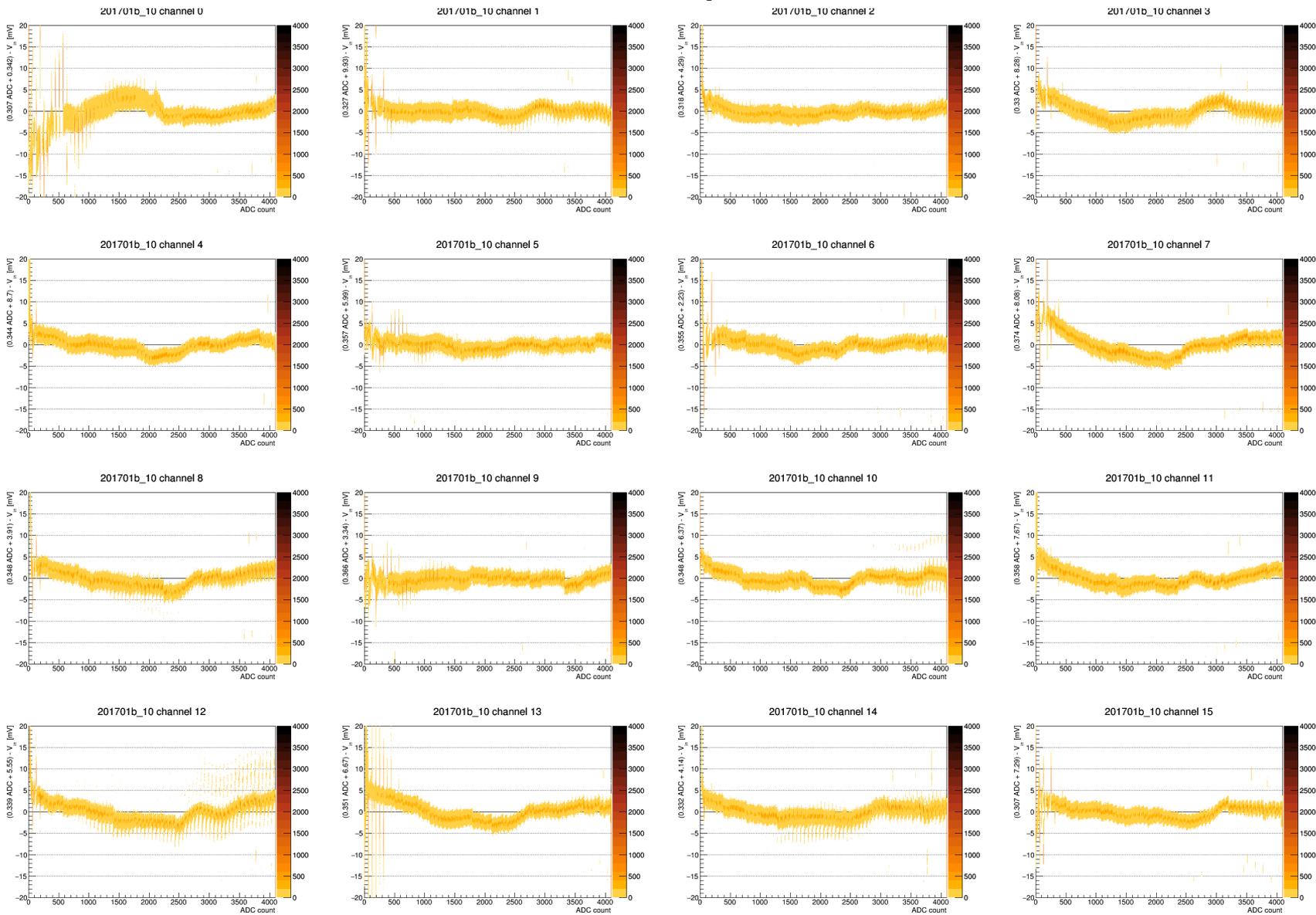
# ADC chip 7



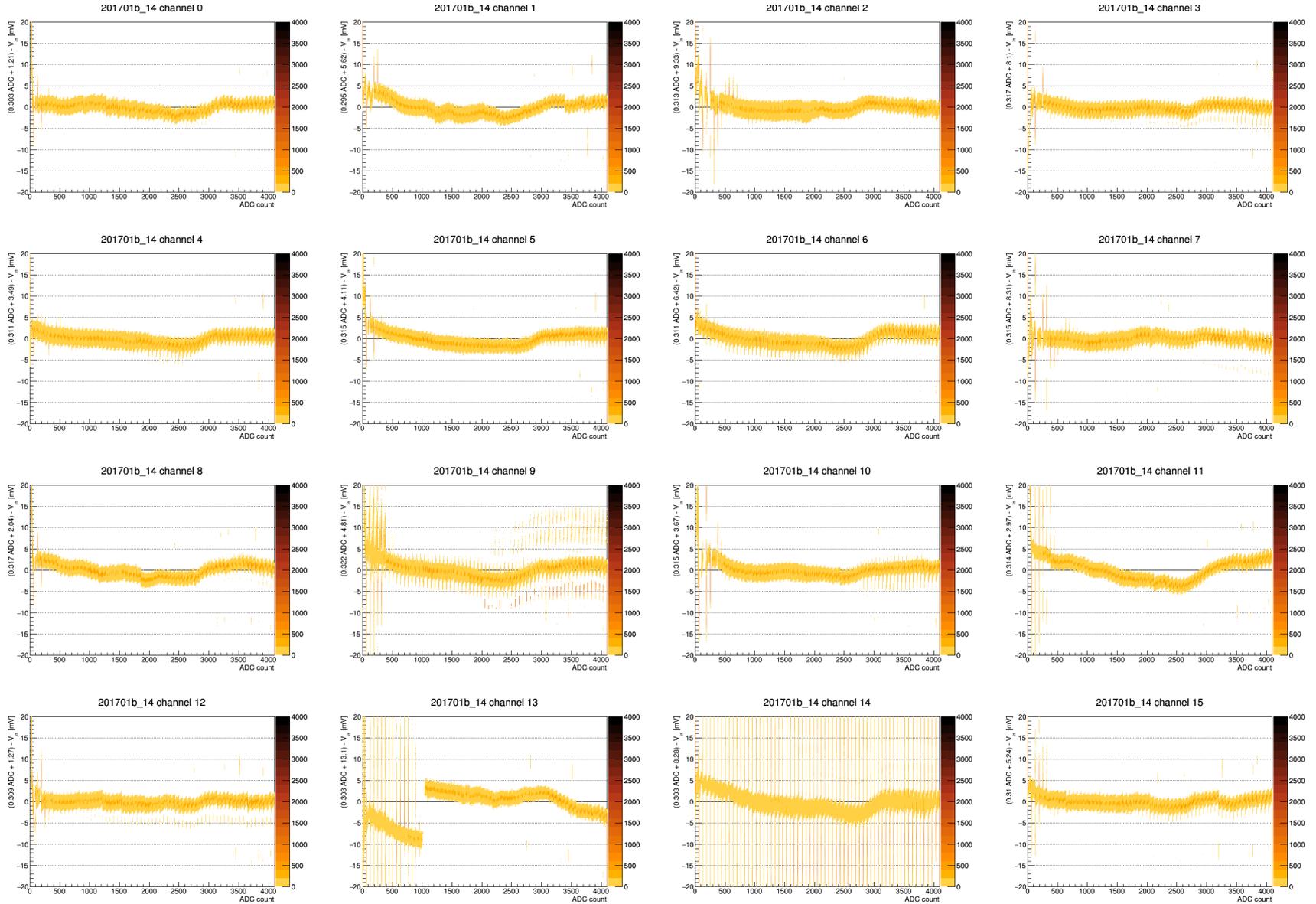
# ADC chip 8



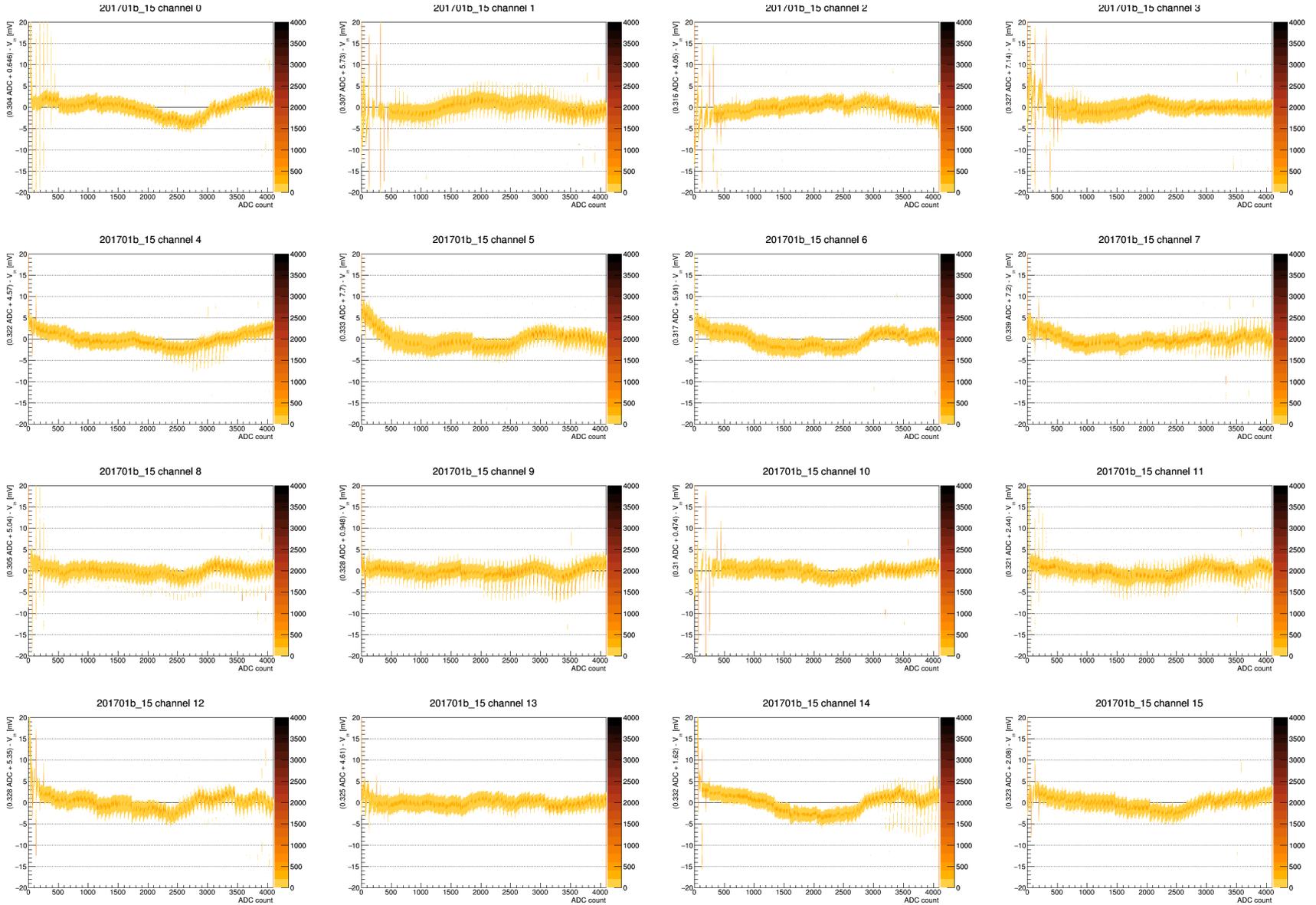
# ADC chip 10



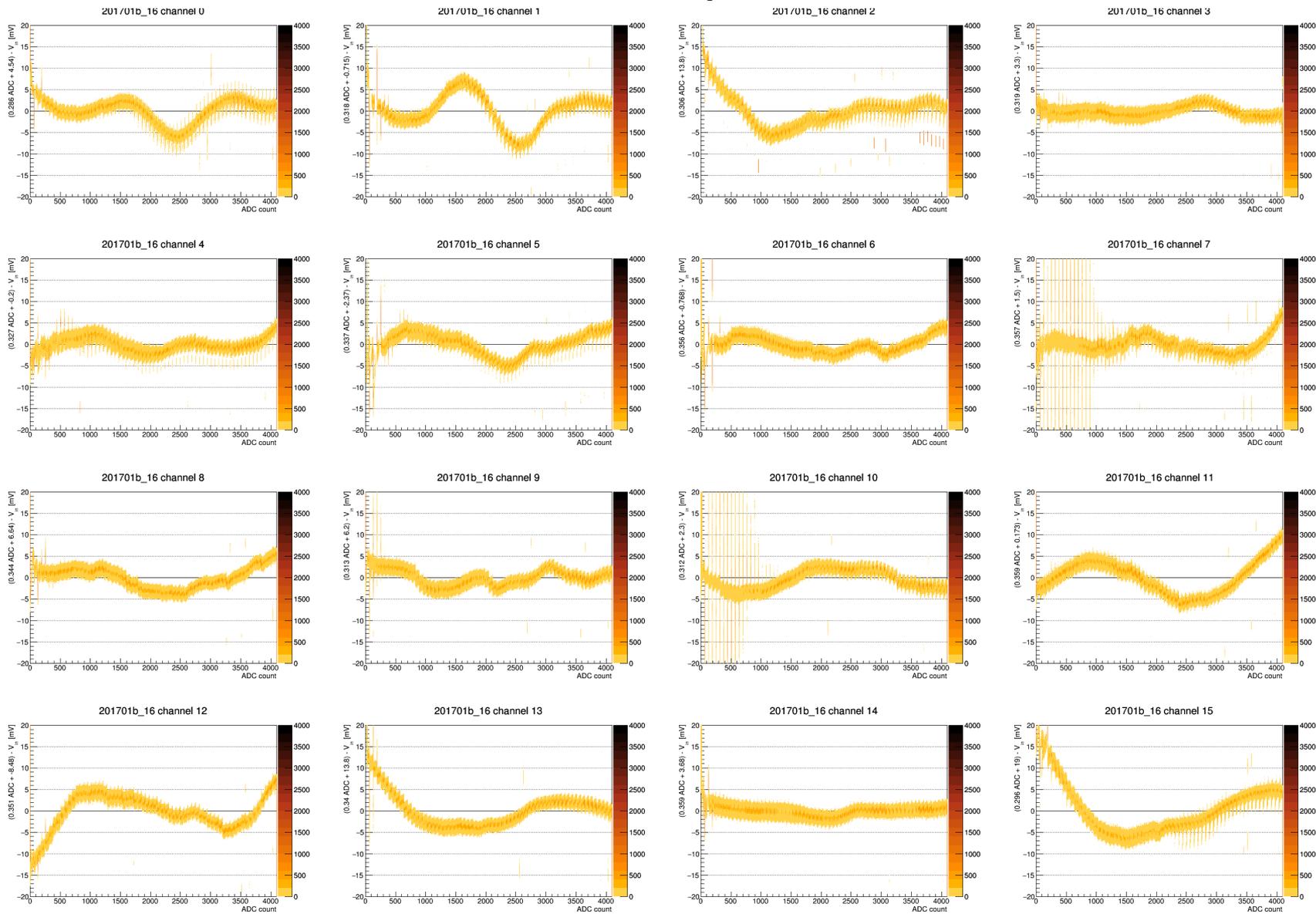
# ADC chip 14



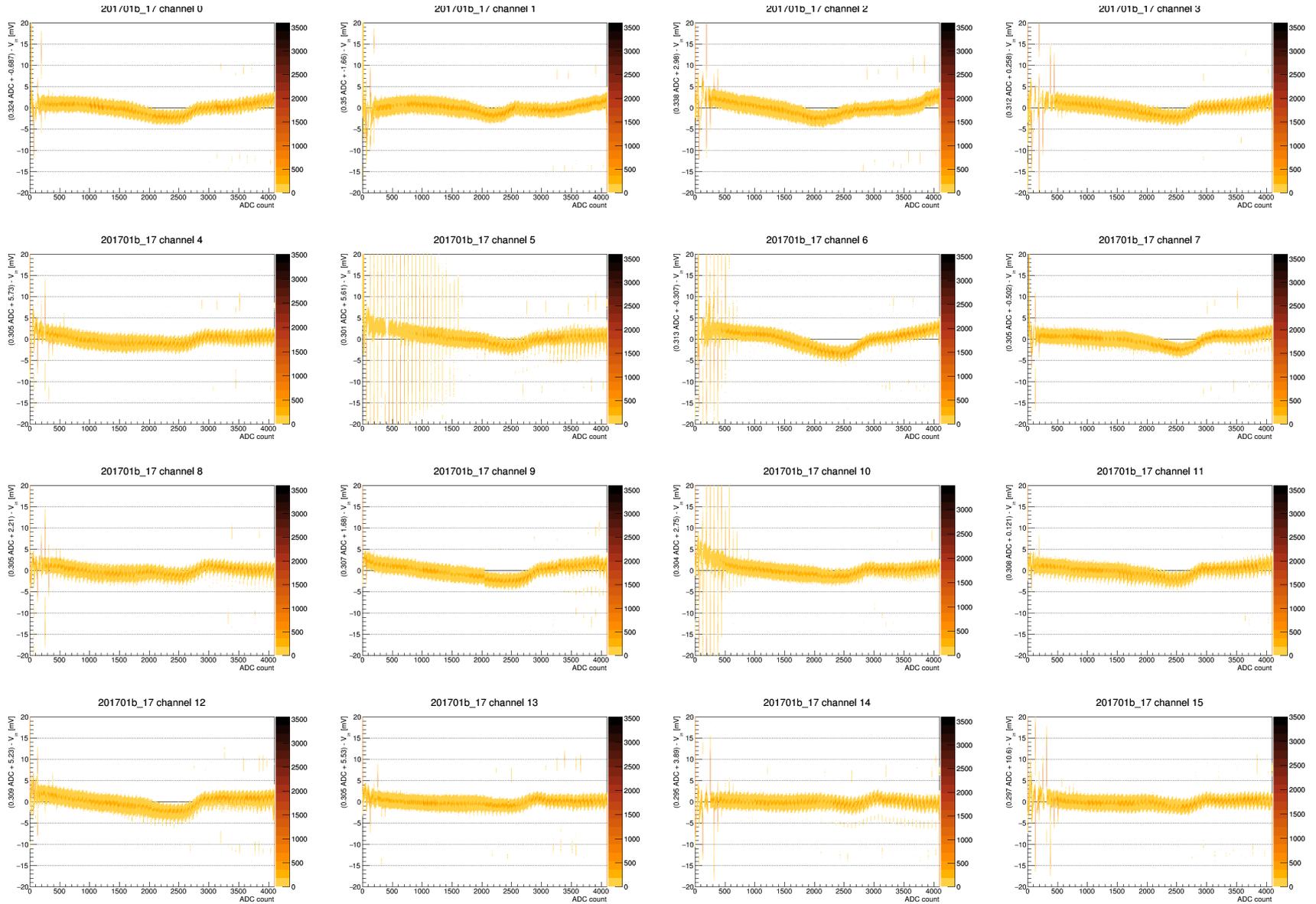
# ADC chip 15



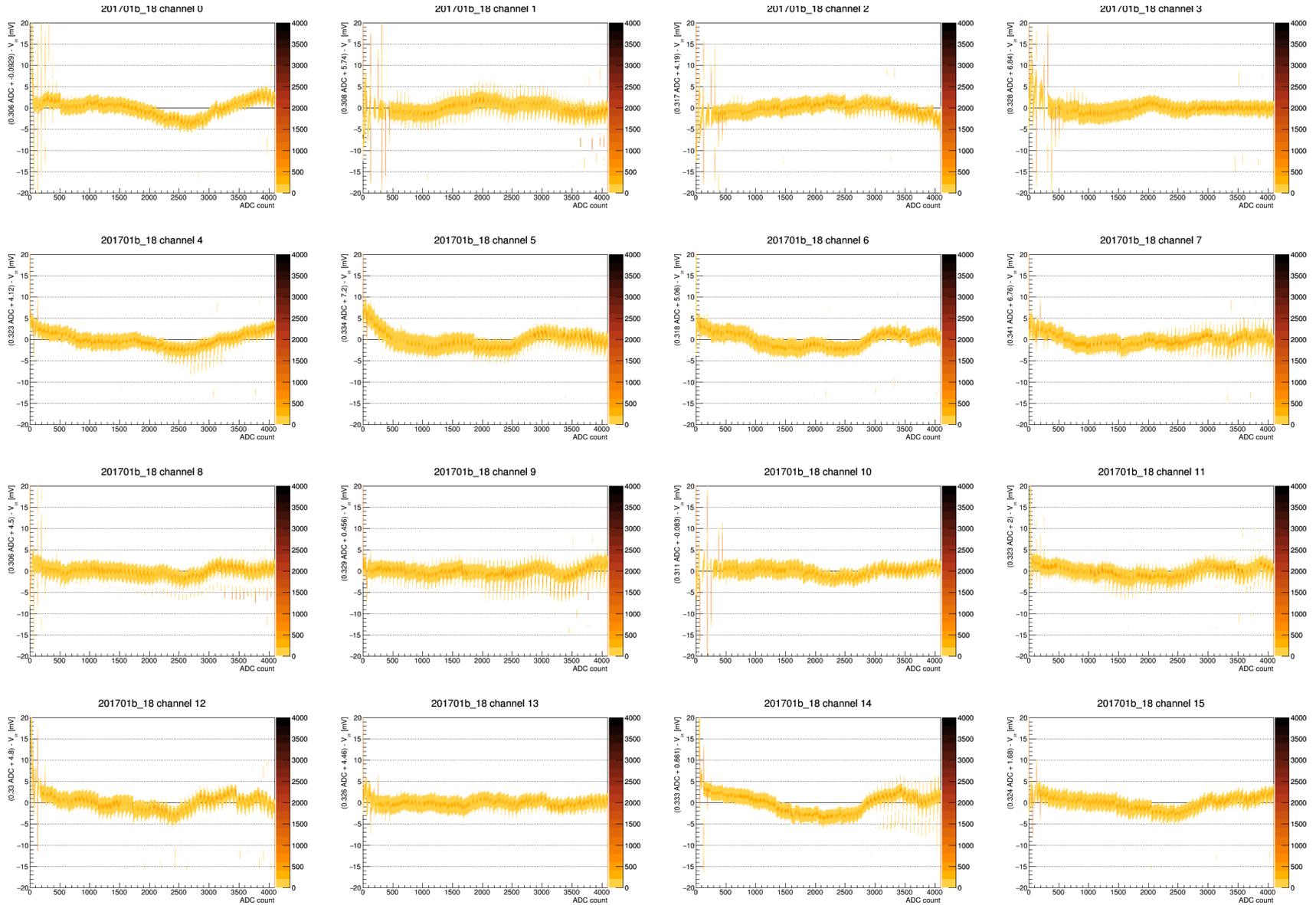
# ADC chip 16



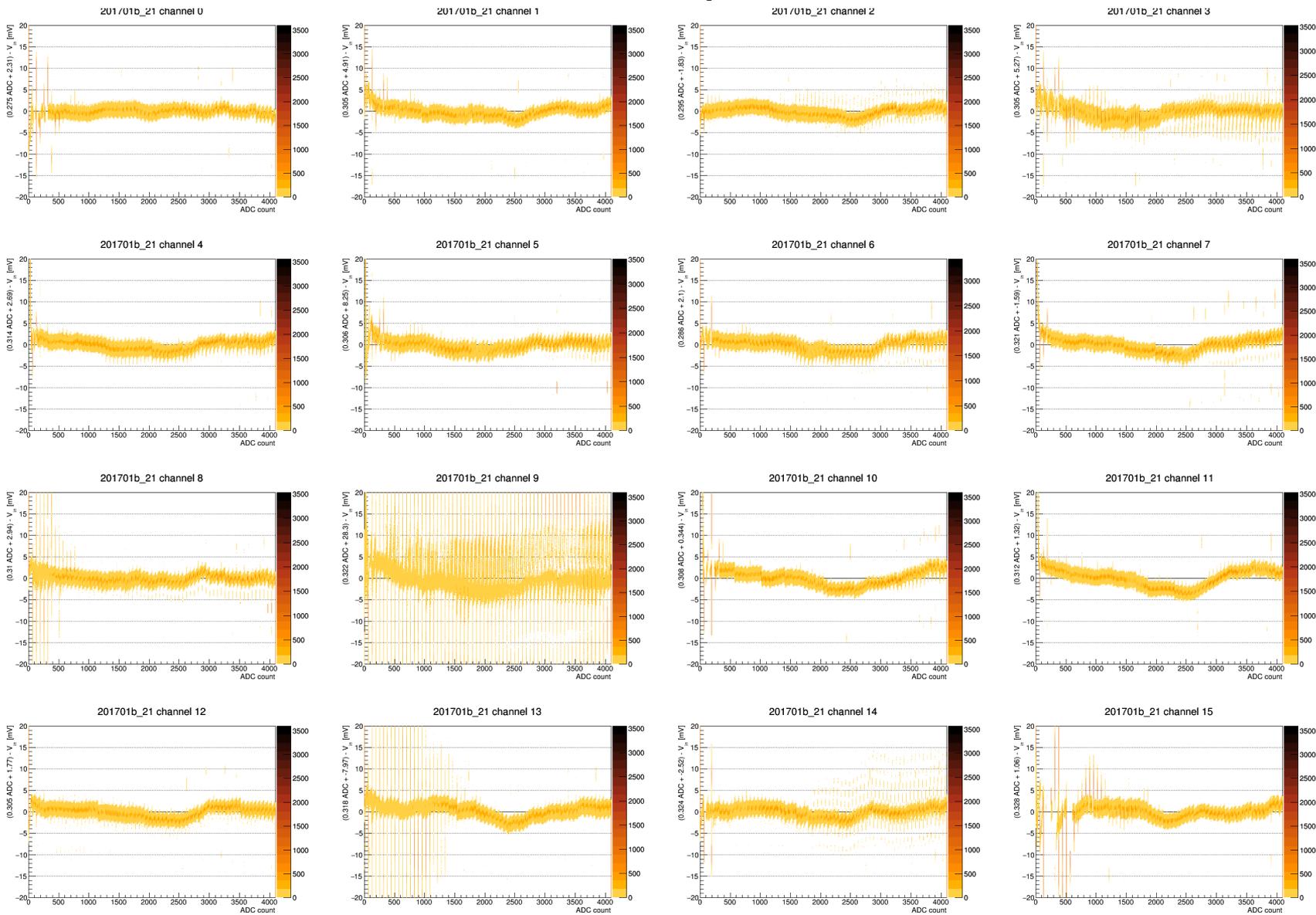
# ADC chip 17



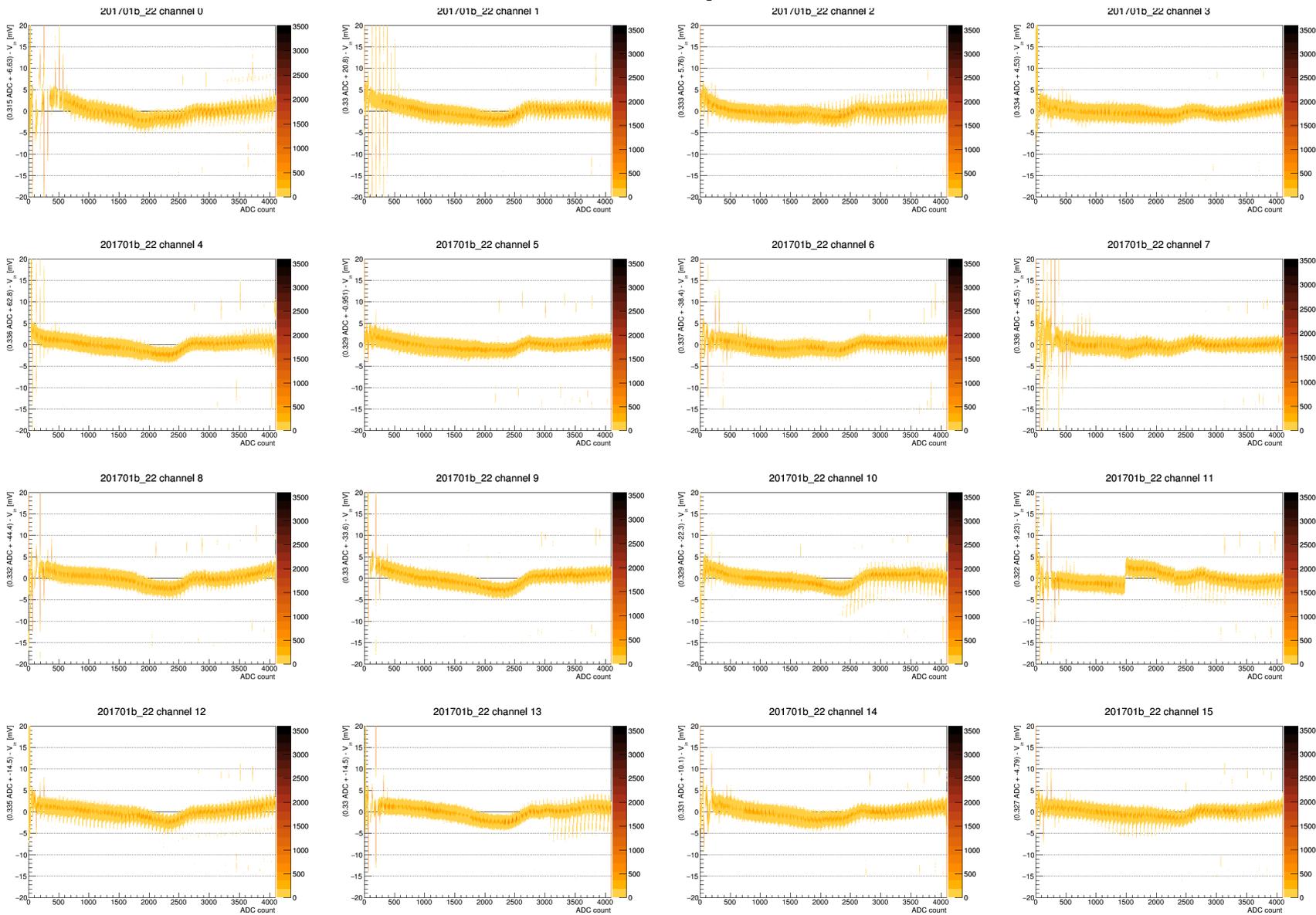
# ADC chip 18



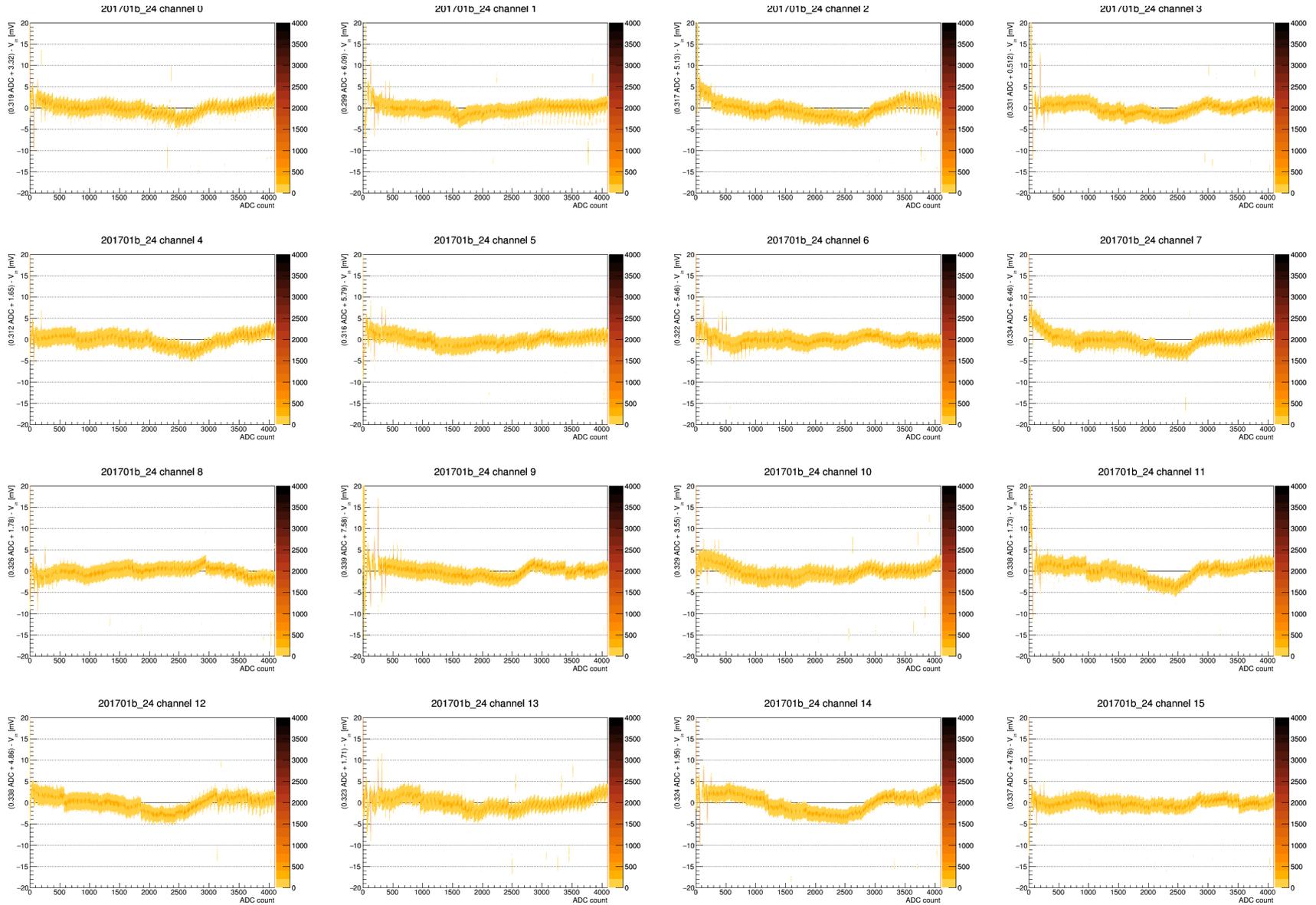
# ADC chip 21



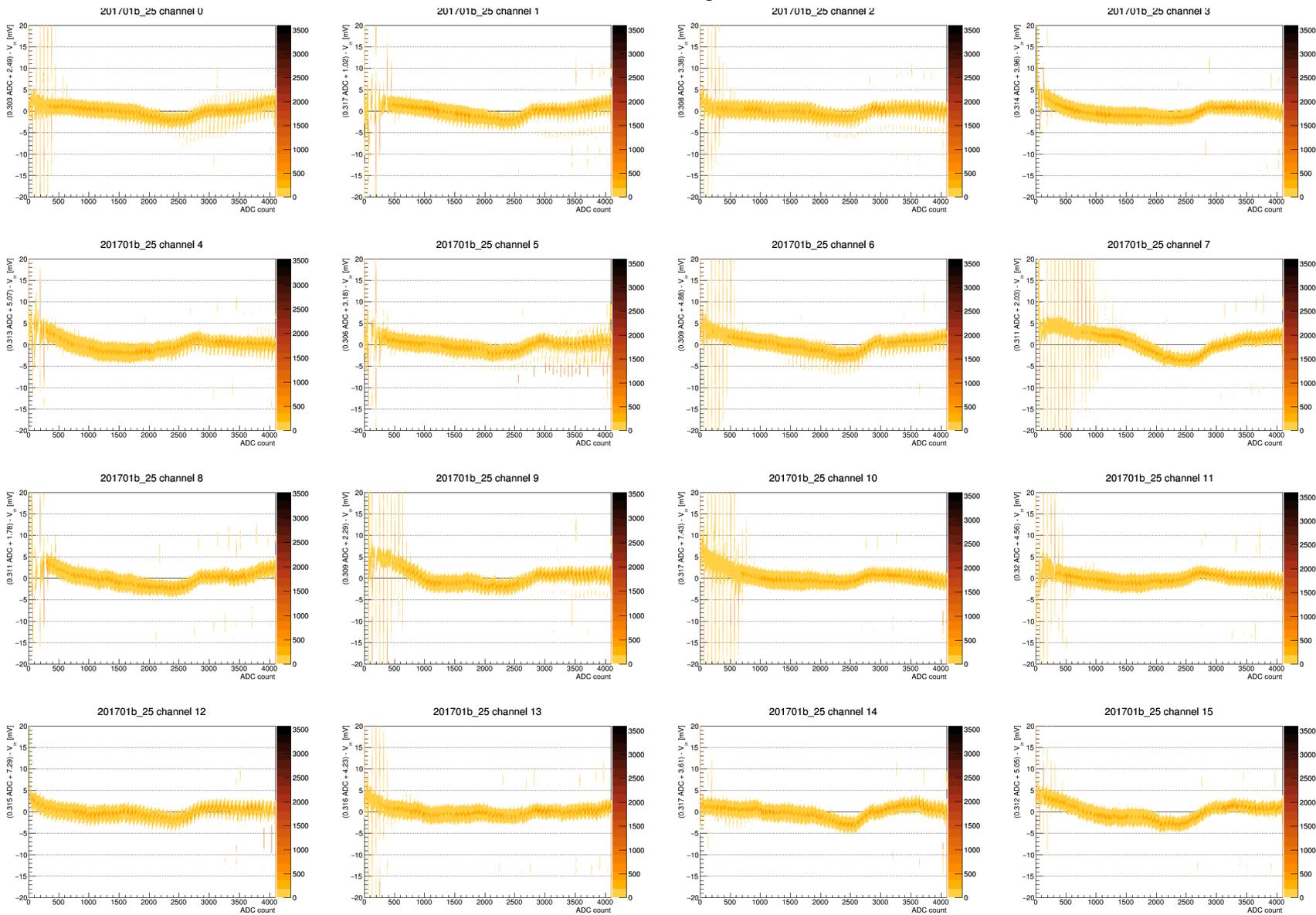
# ADC chip 22



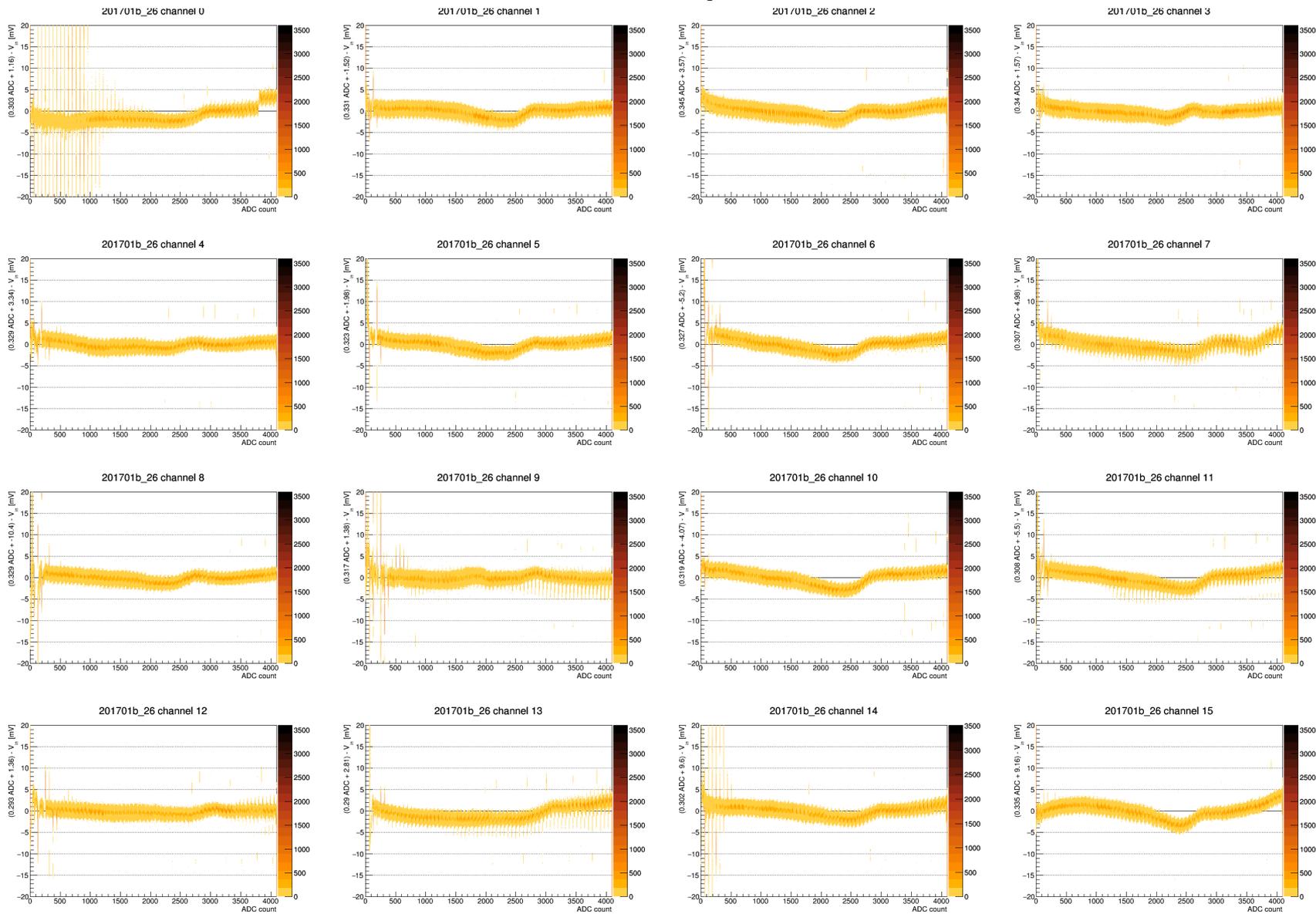
# ADC chip 24



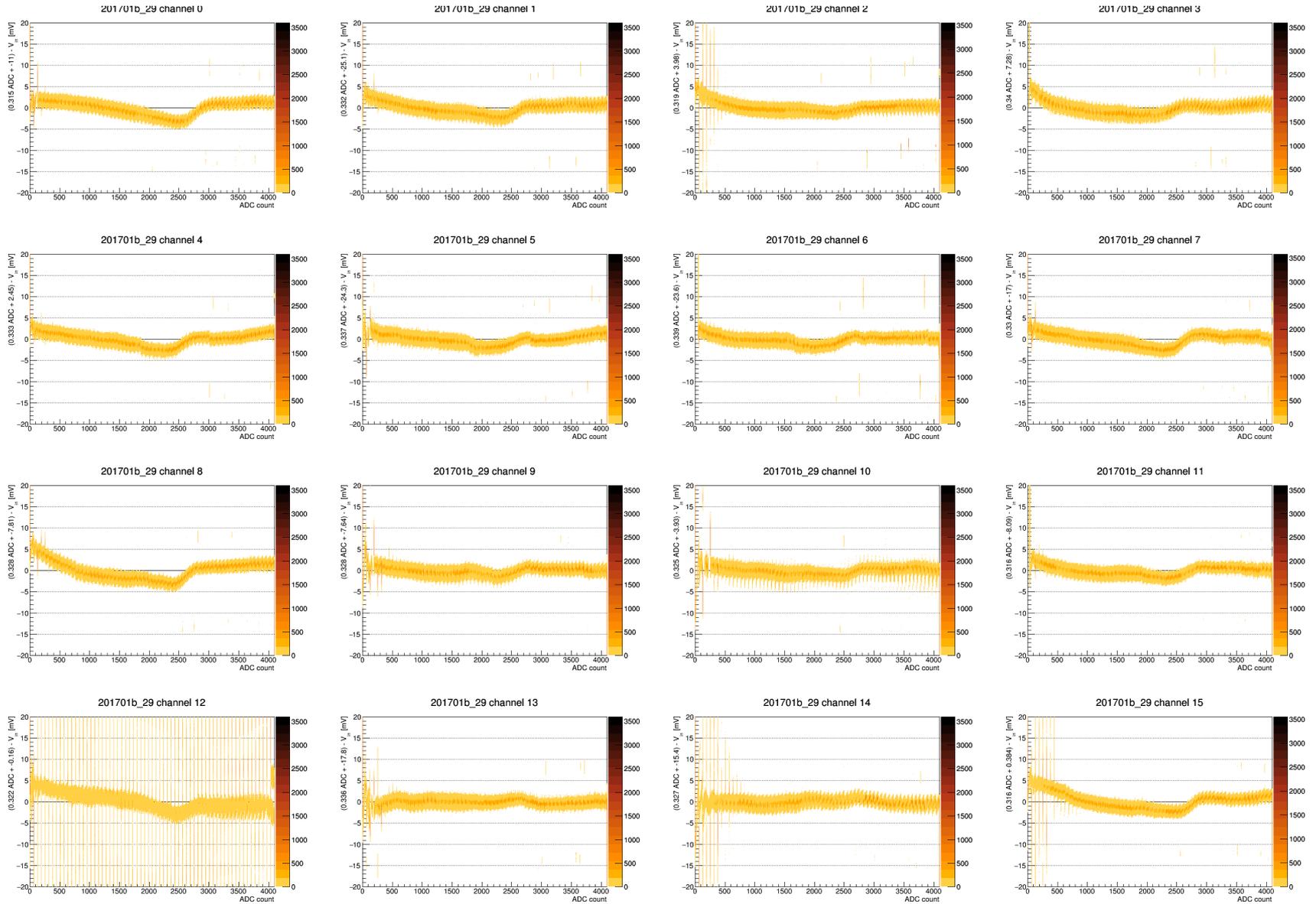
# ADC chip 25



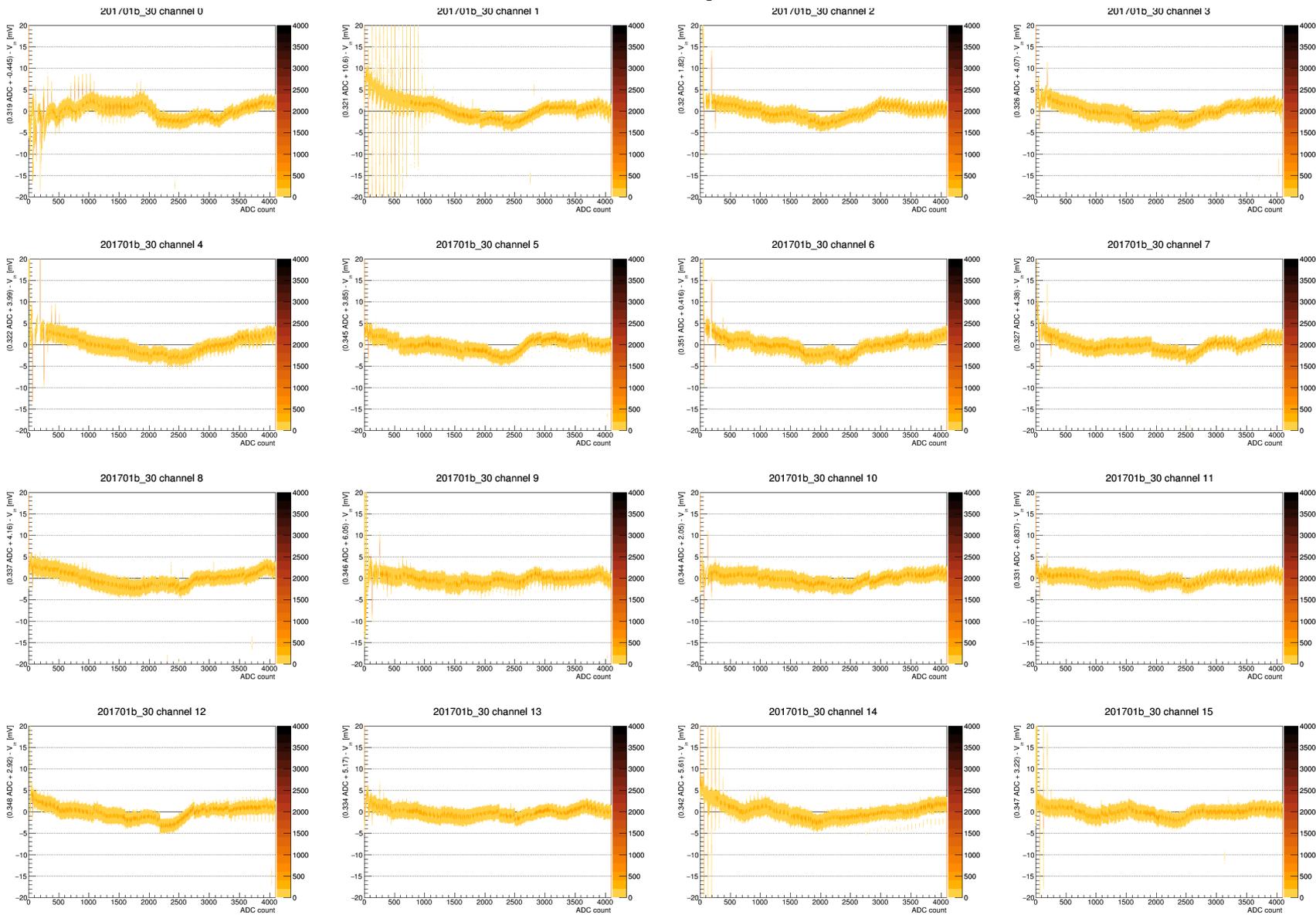
# ADC chip 26



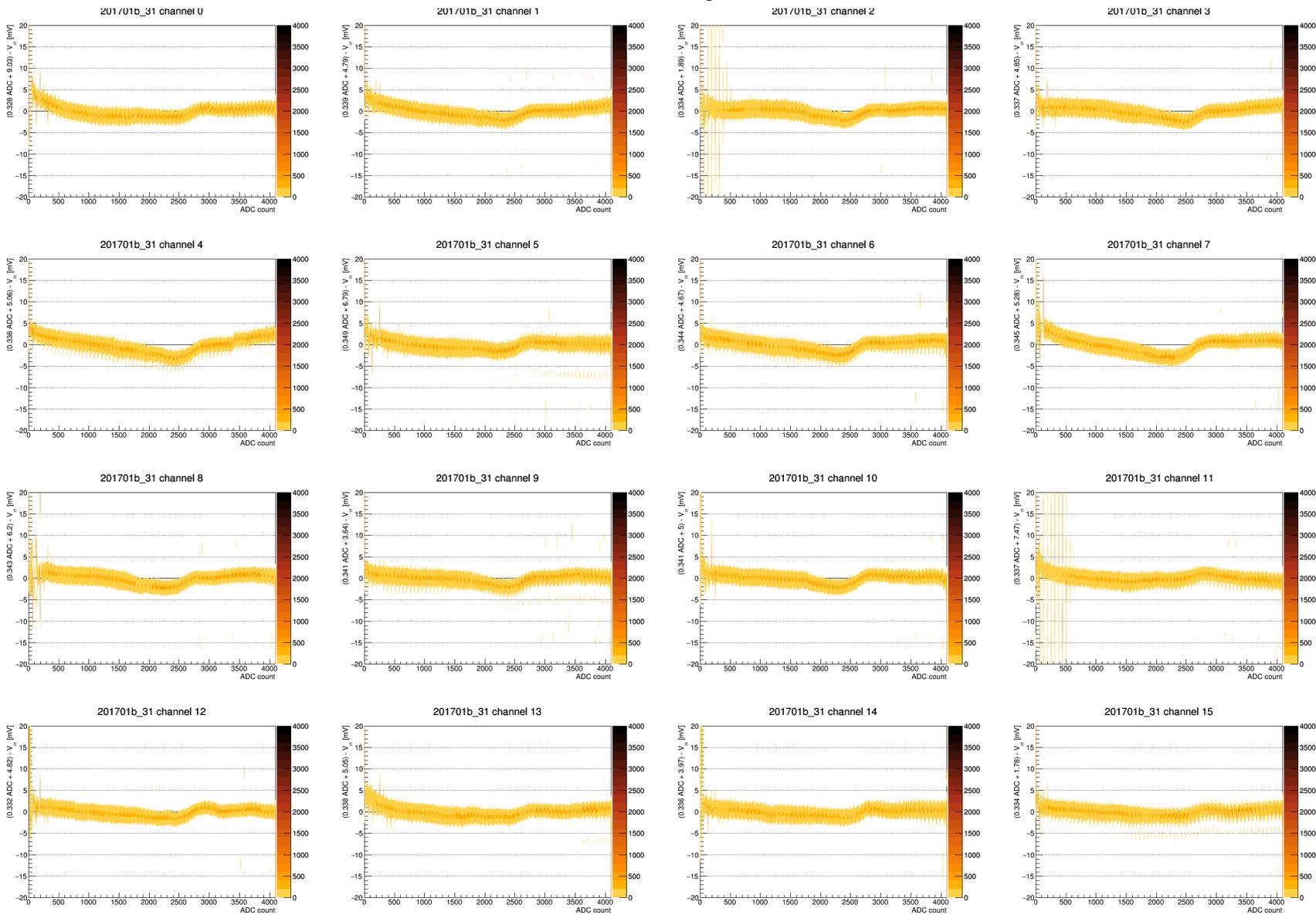
# ADC chip 29



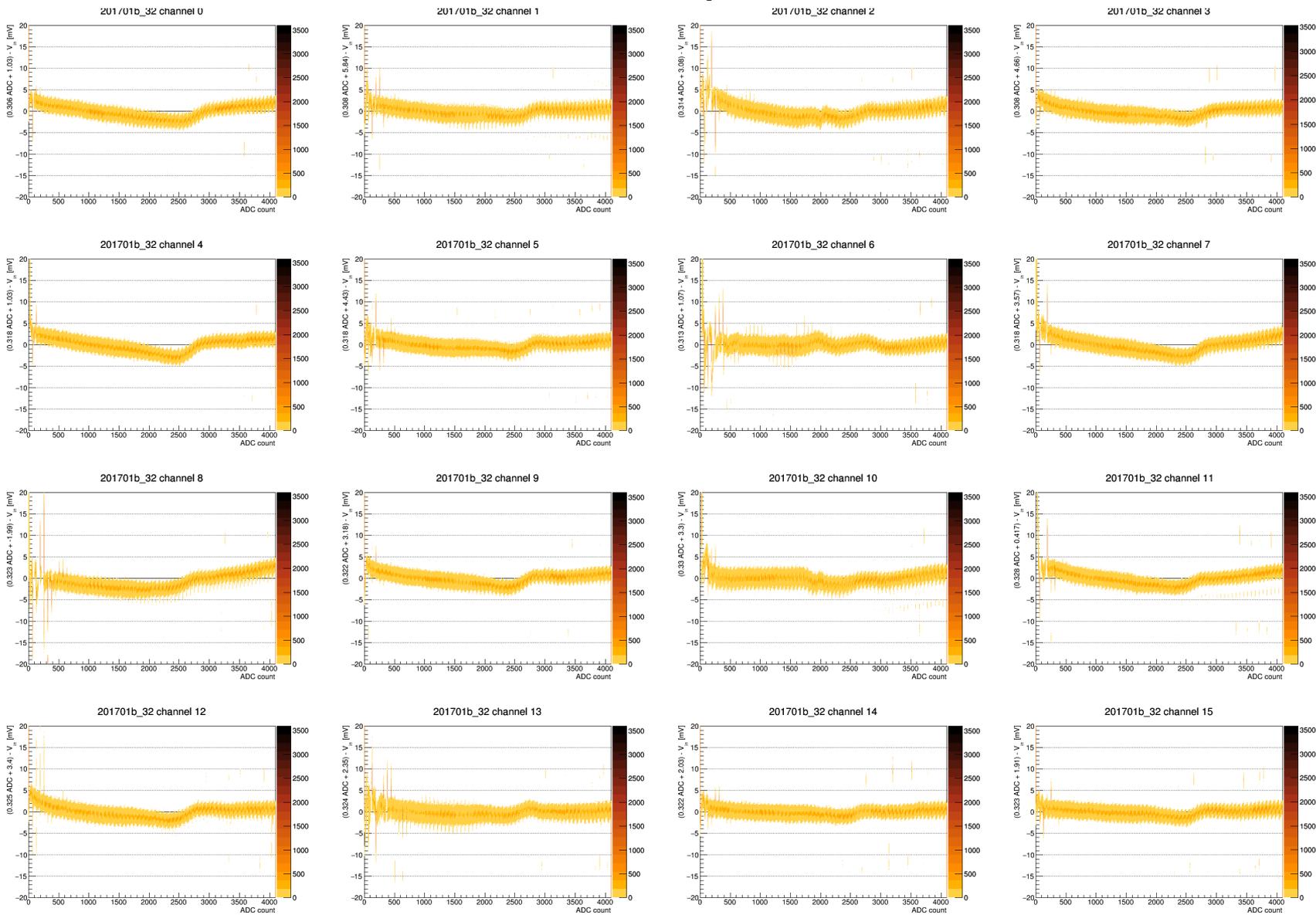
# ADC chip 30



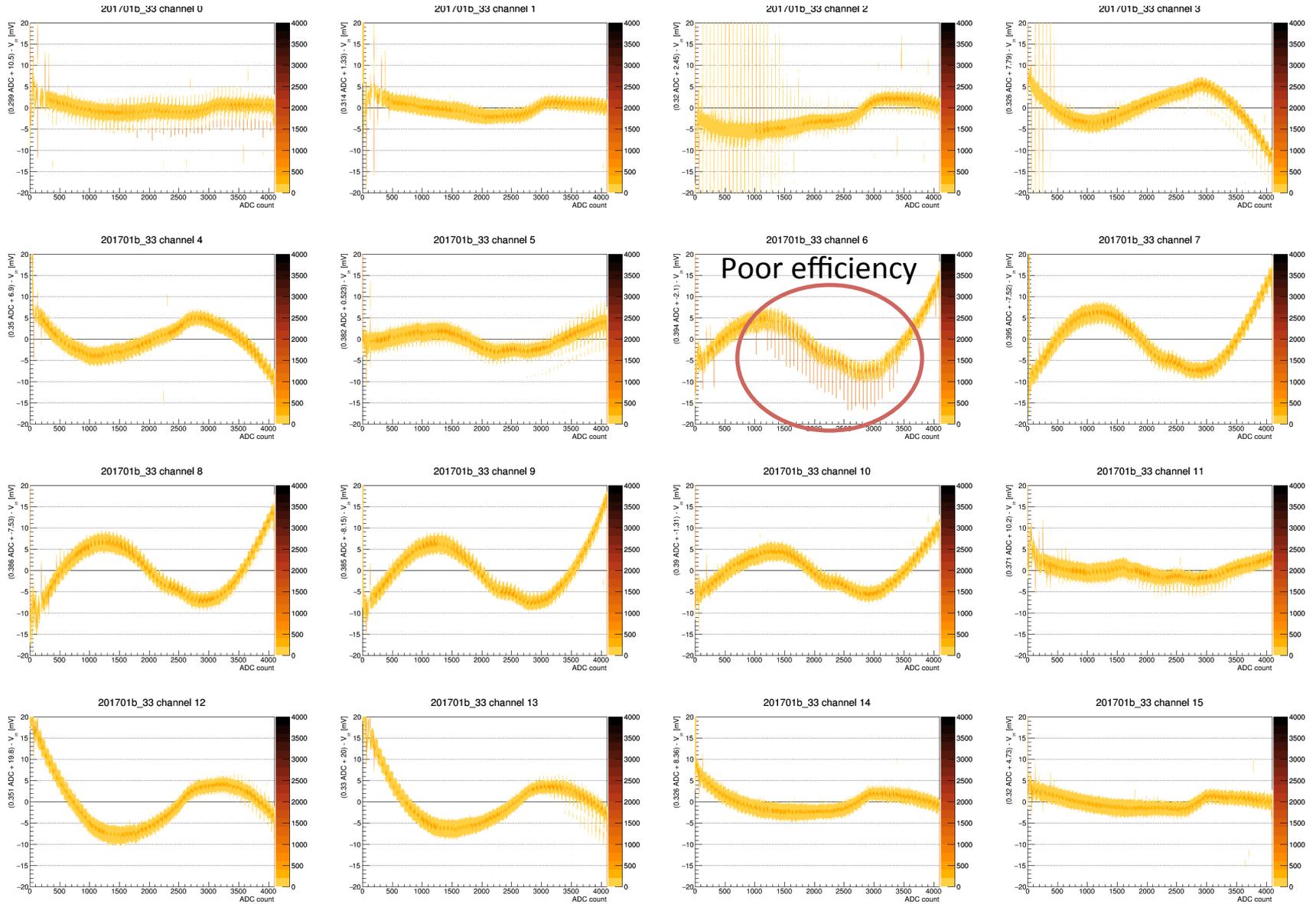
# ADC chip 31



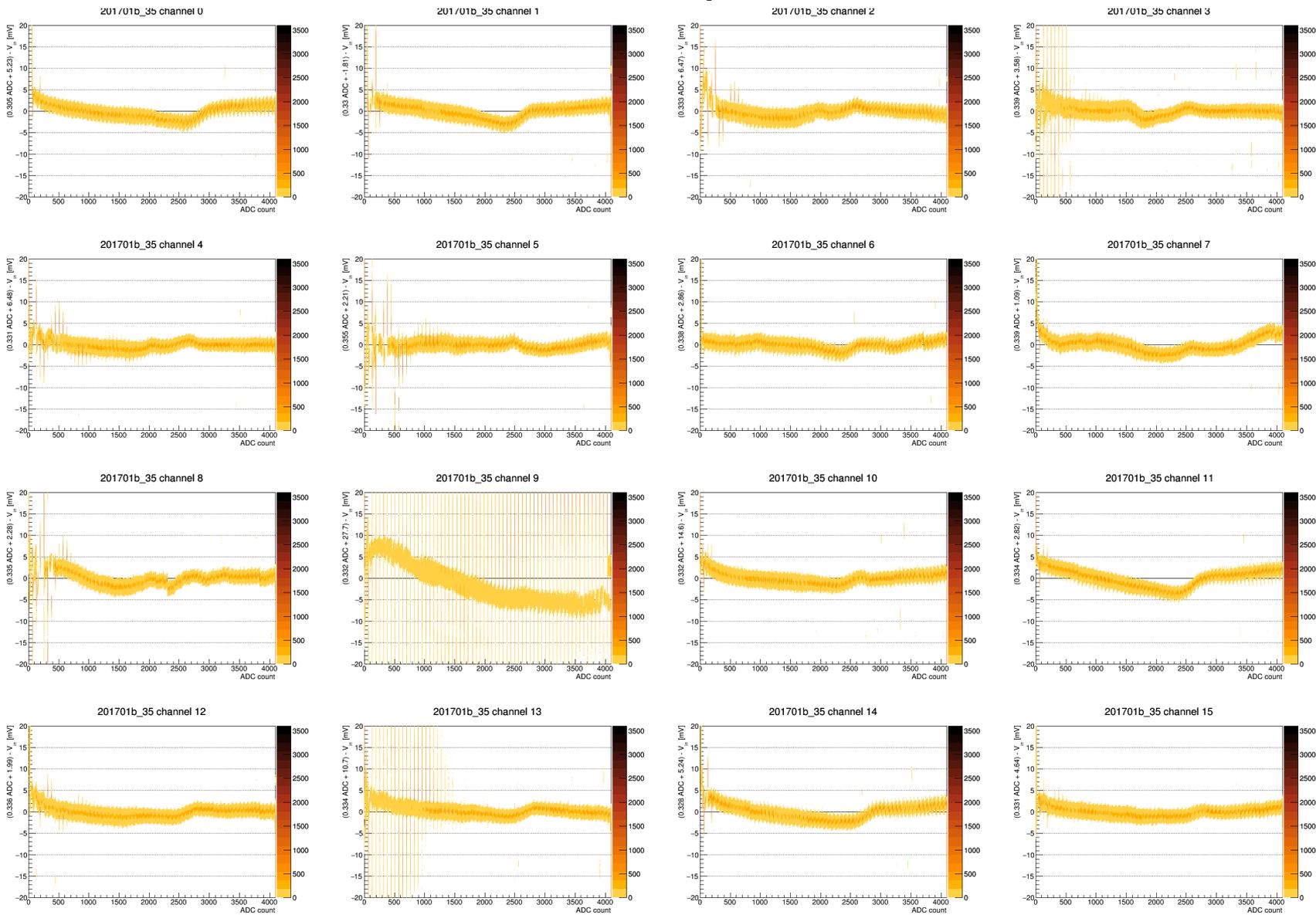
# ADC chip 32



# ADC chip 33



# ADC chip 35

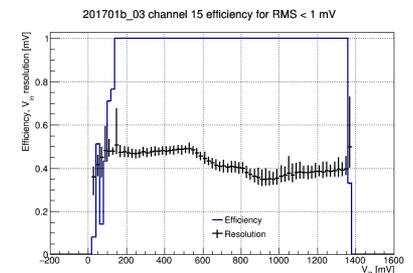
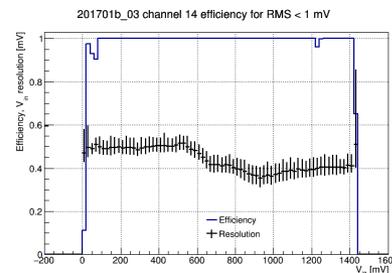
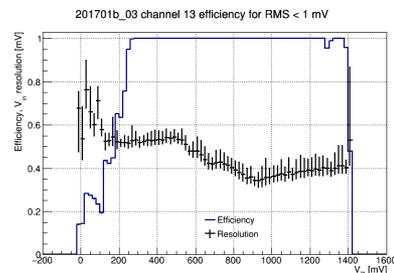
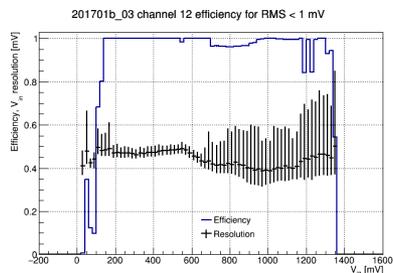
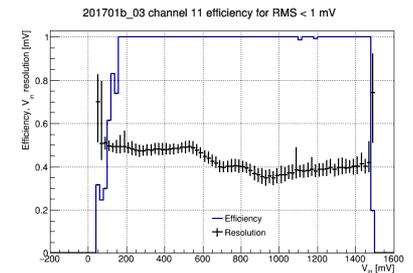
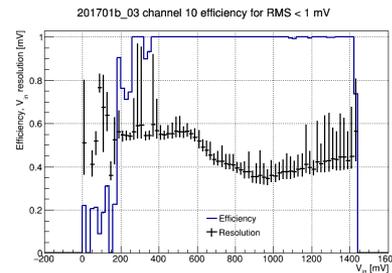
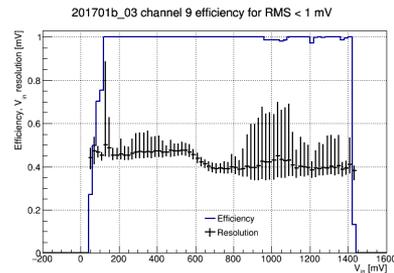
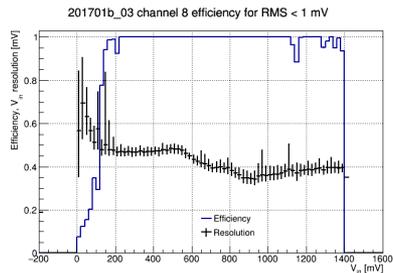
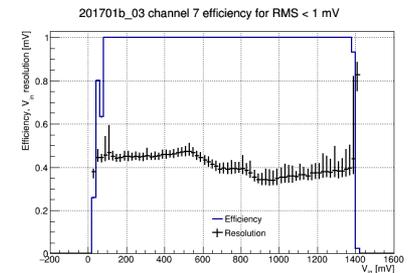
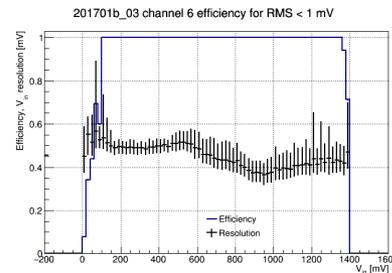
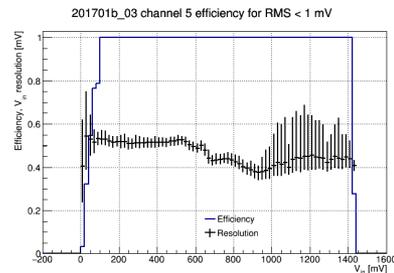
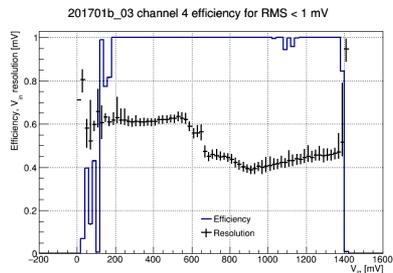
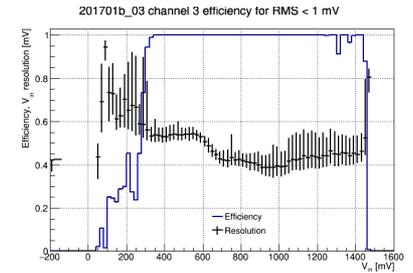
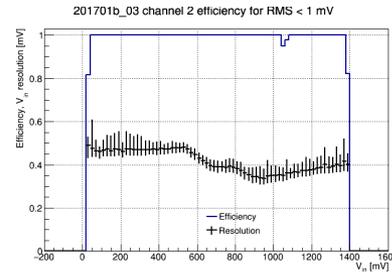
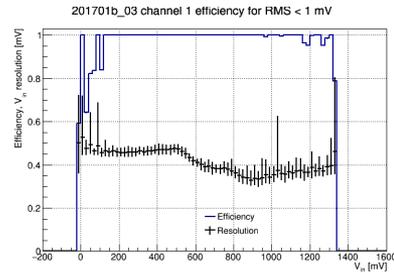
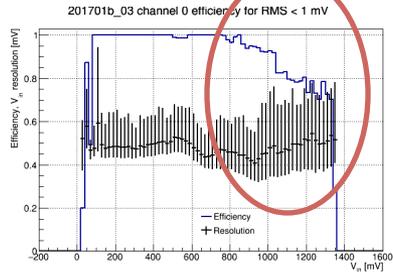


## Efficiency vs. $V_{in}$ for all channels





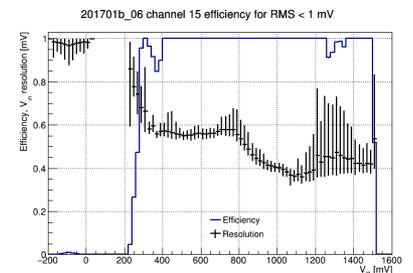
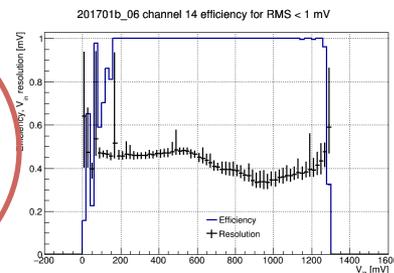
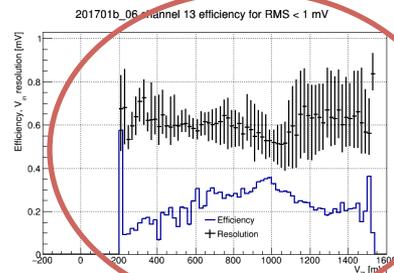
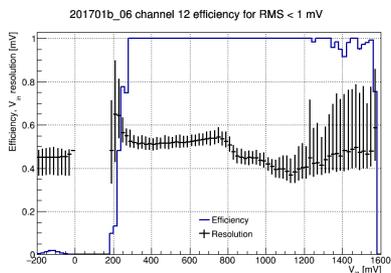
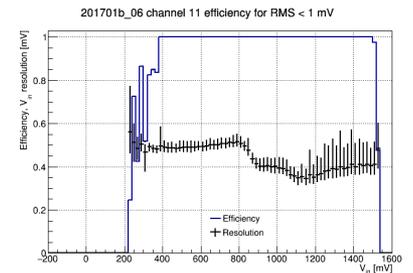
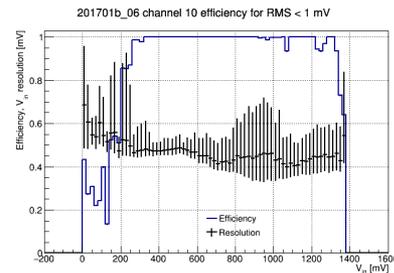
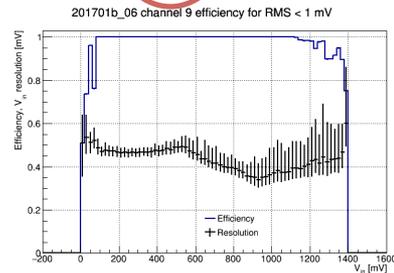
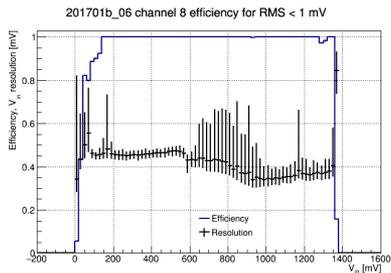
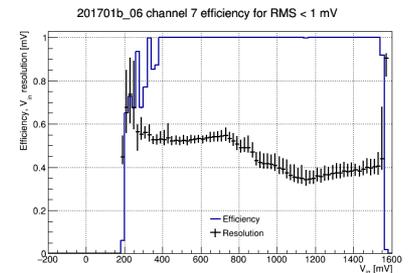
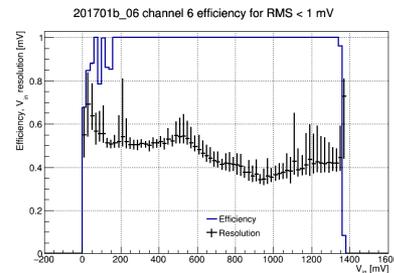
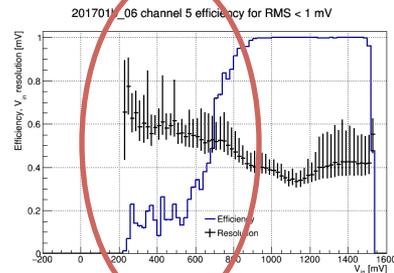
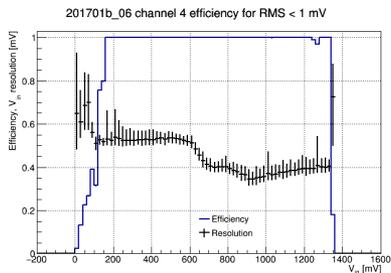
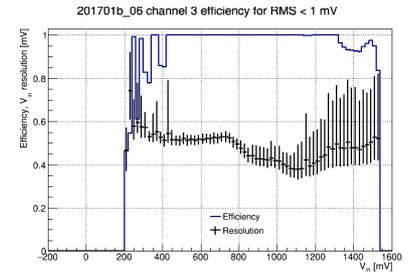
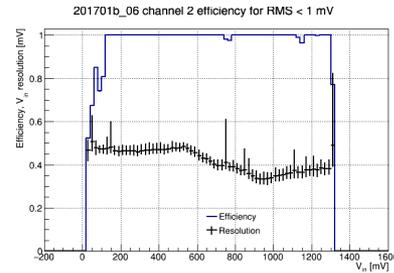
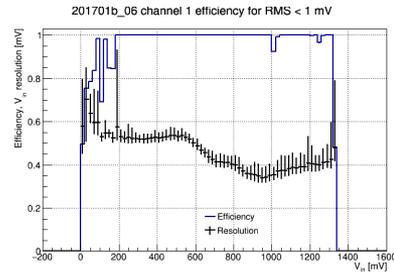
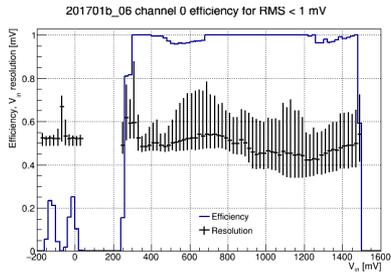
# ADC chip 3 (poor)



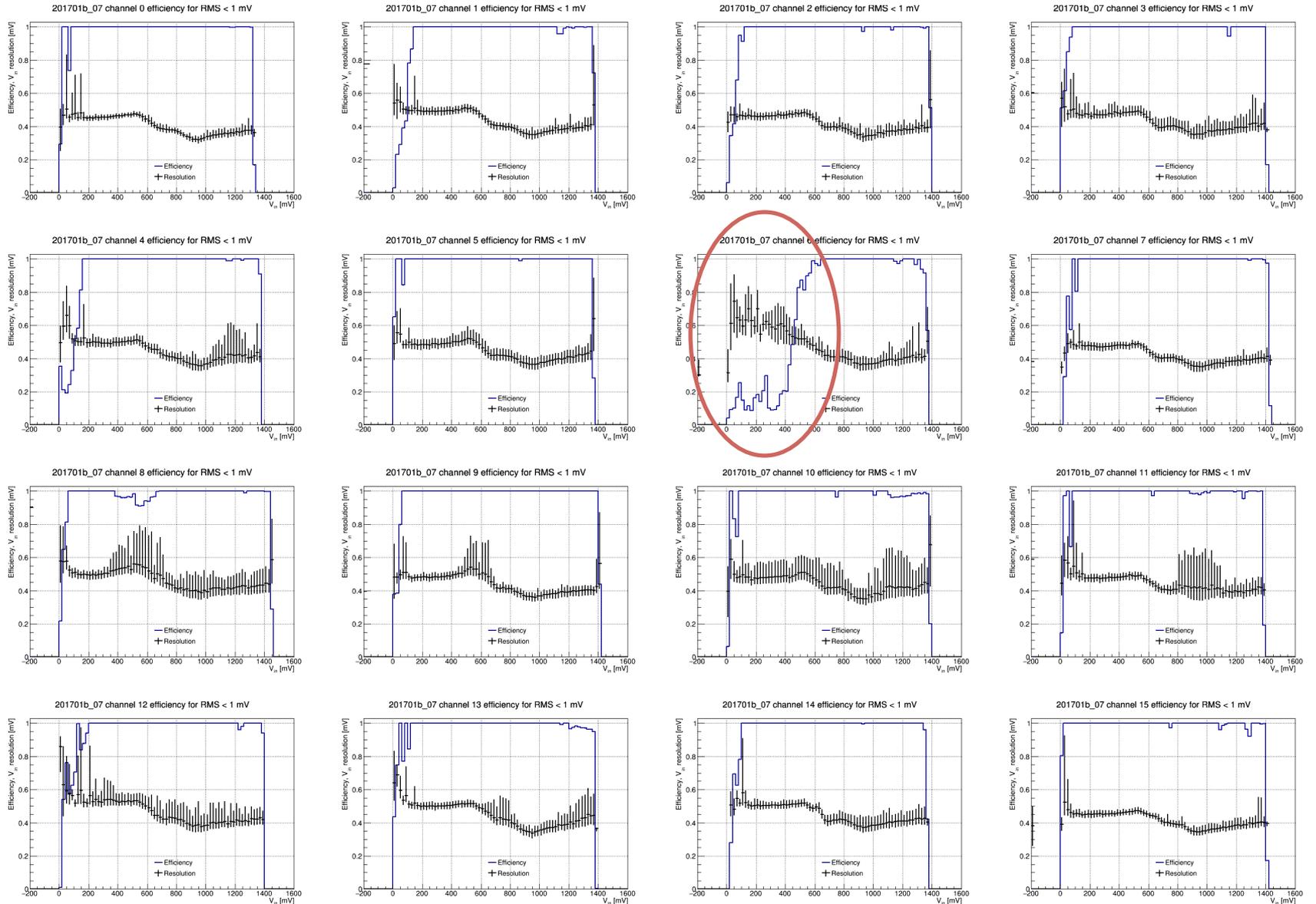




# ADC chip 6 (bad)



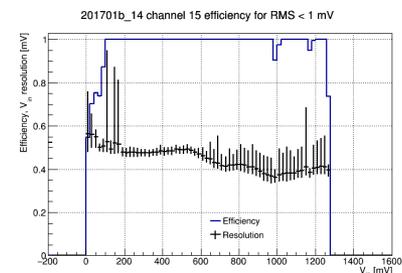
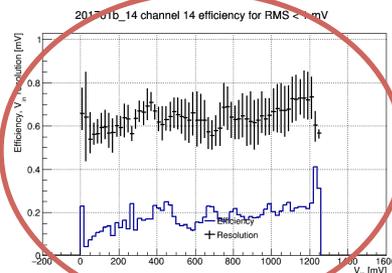
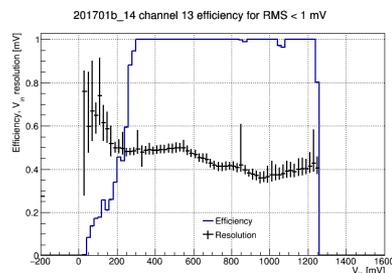
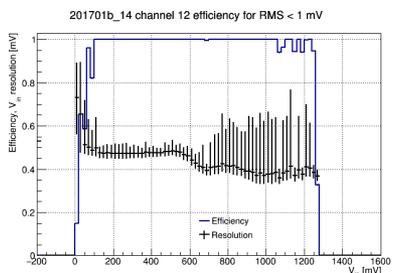
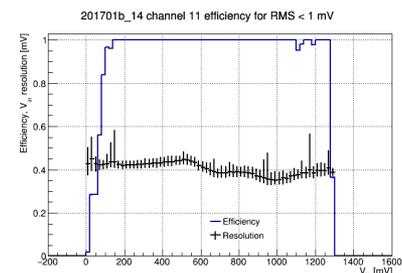
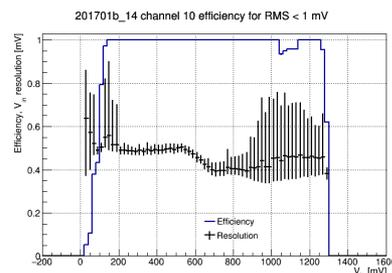
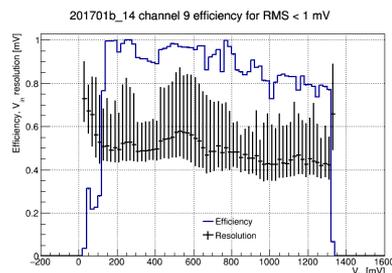
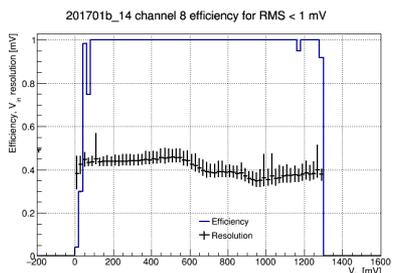
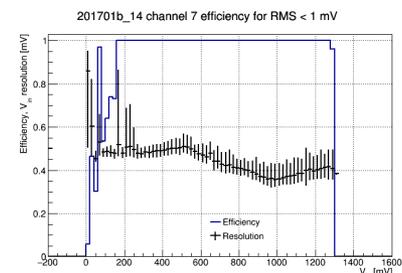
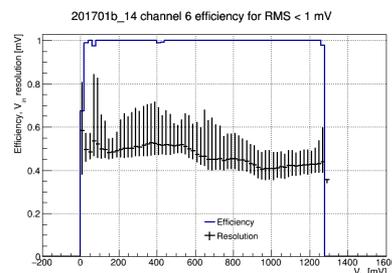
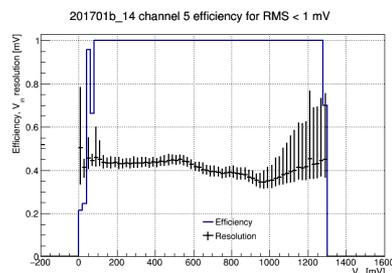
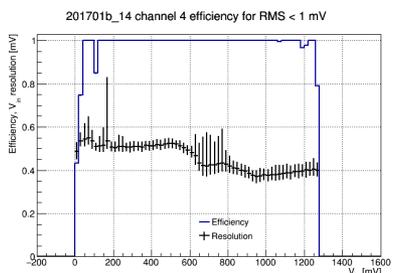
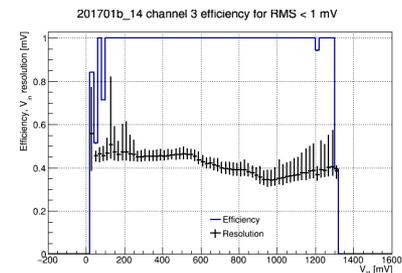
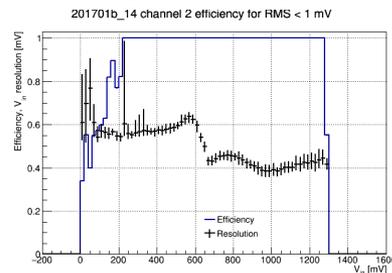
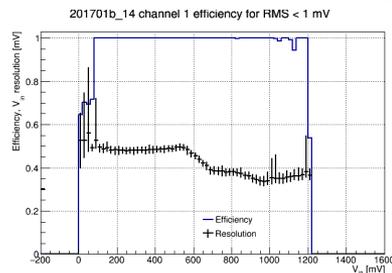
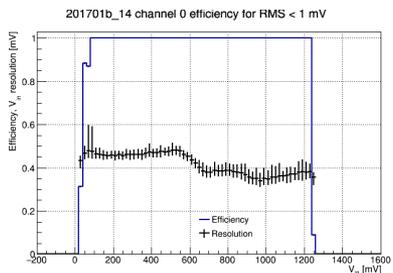
# ADC chip 7 (poor)



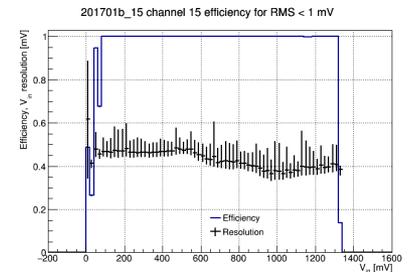
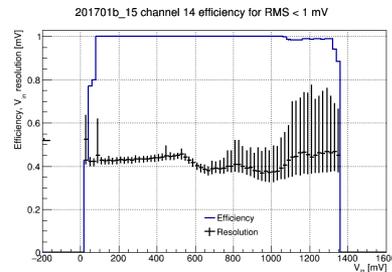
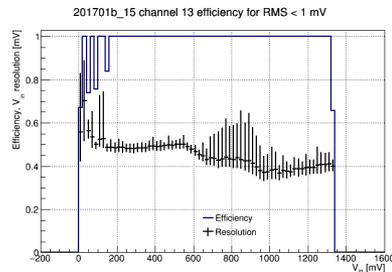
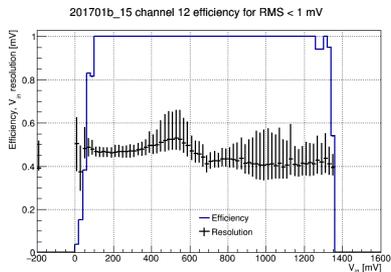
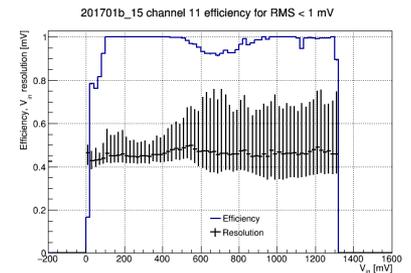
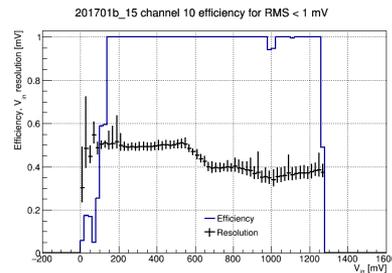
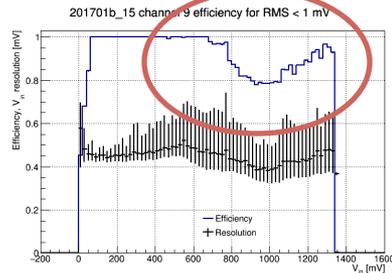
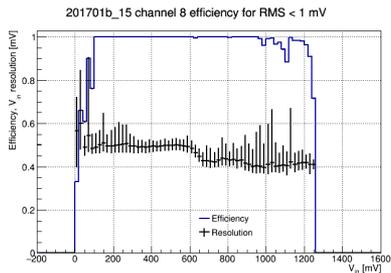
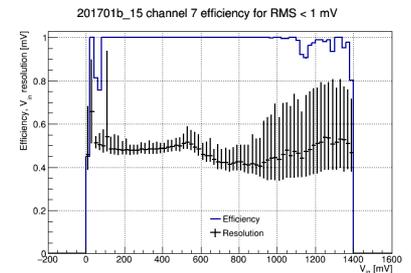
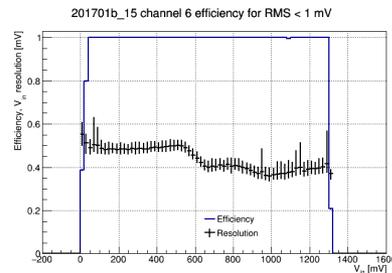
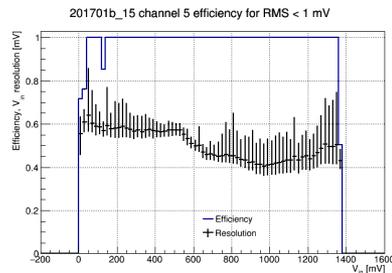
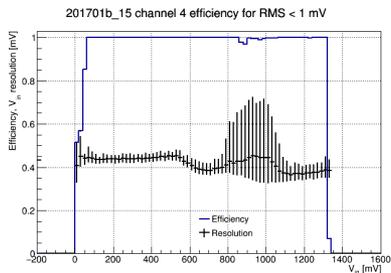
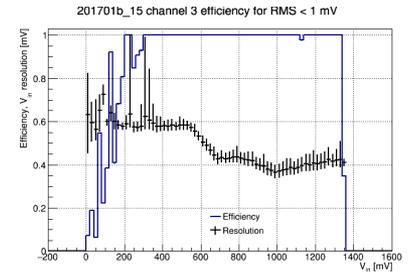
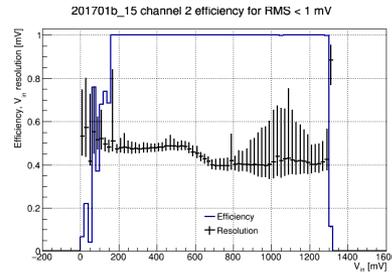
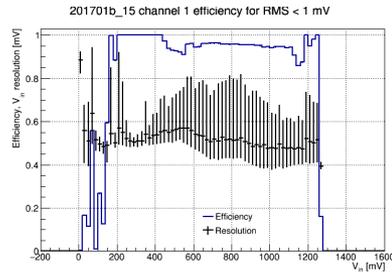
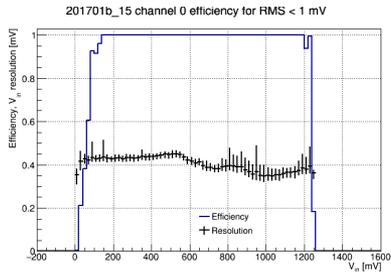




# ADC chip 14 (bad)

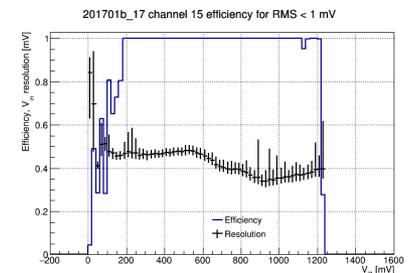
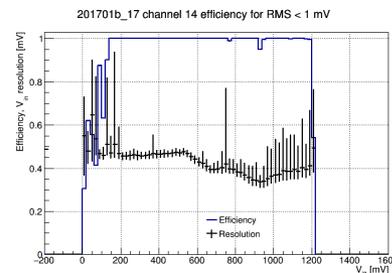
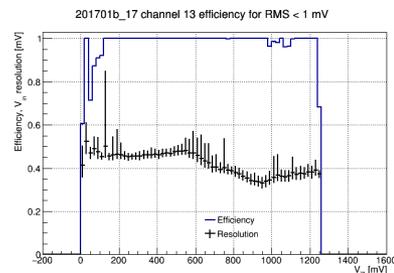
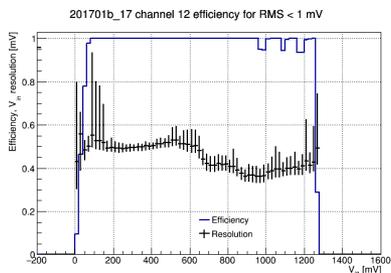
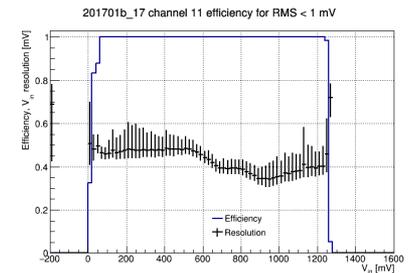
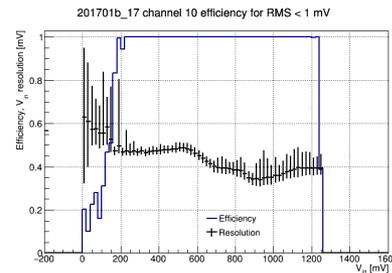
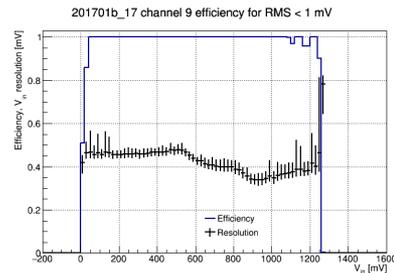
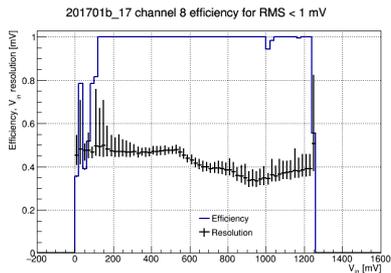
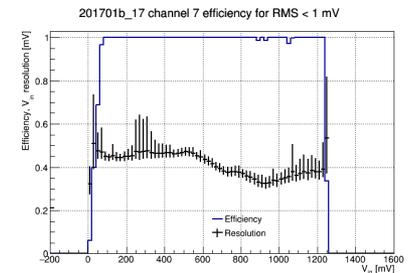
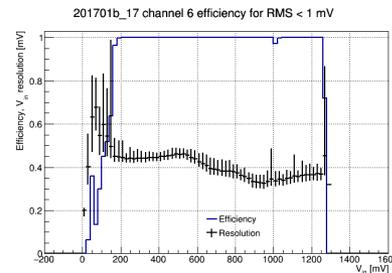
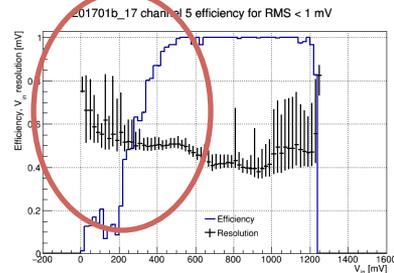
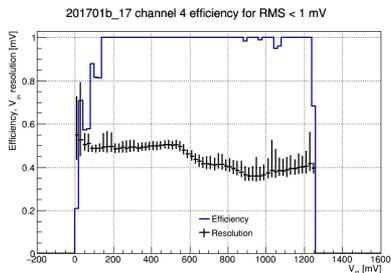
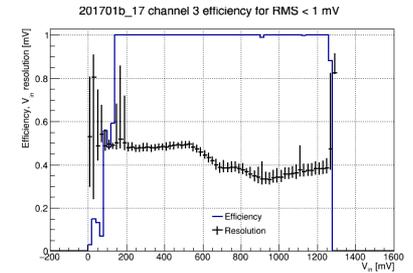
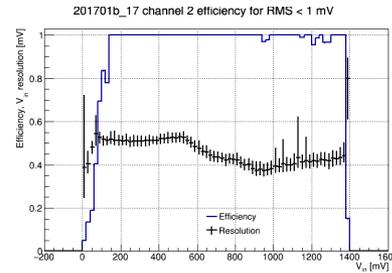
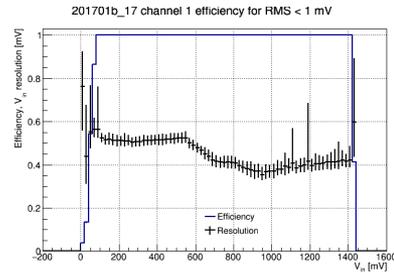
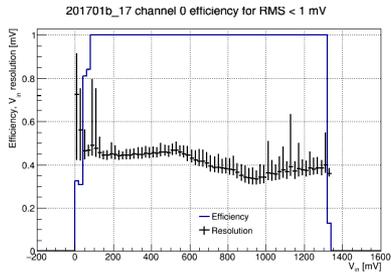


# ADC chip 15 (poor)

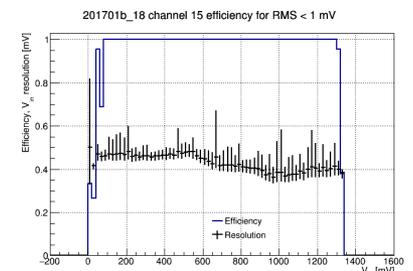
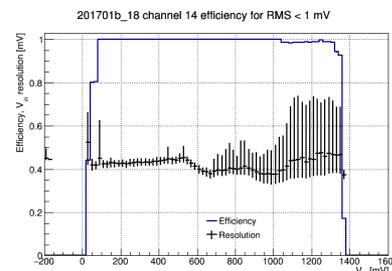
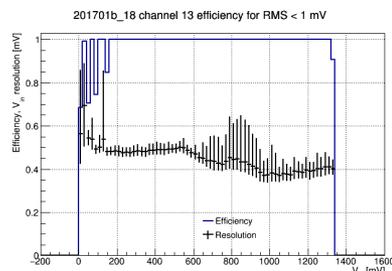
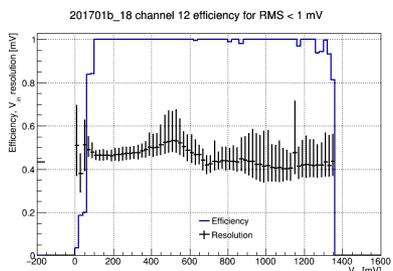
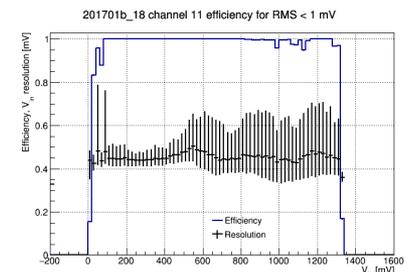
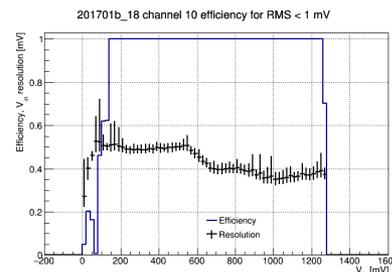
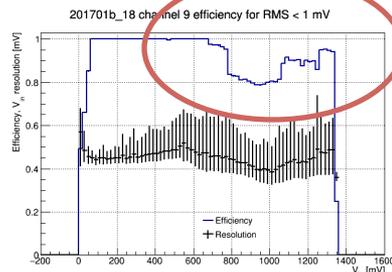
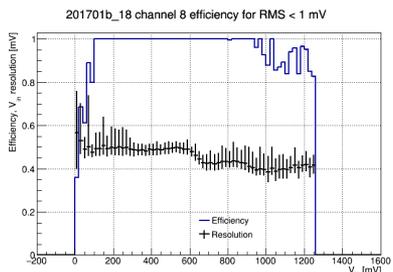
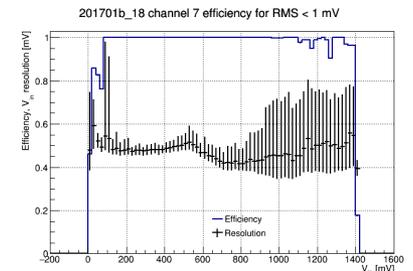
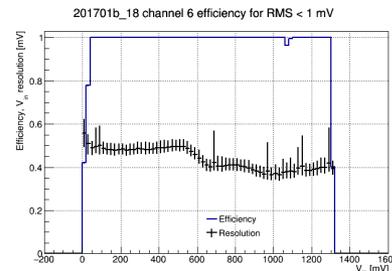
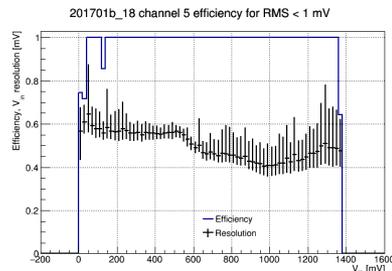
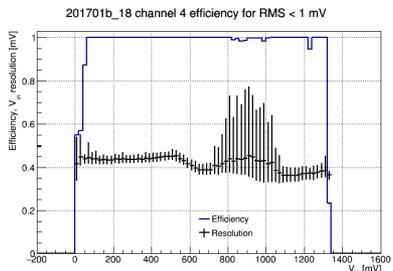
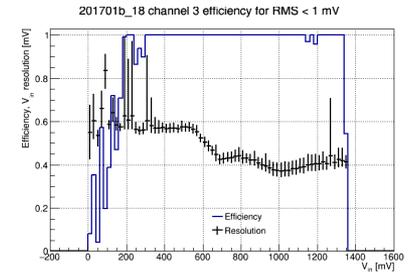
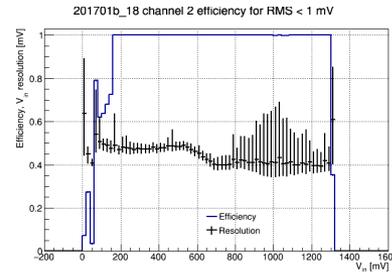
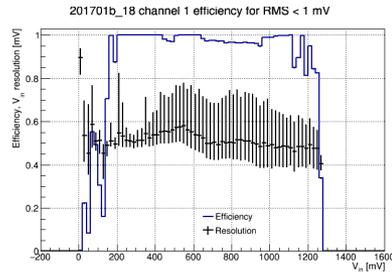
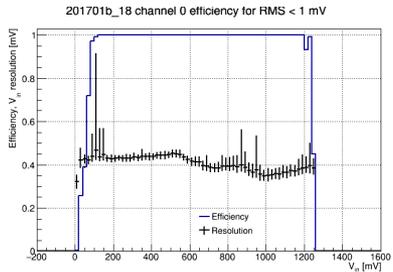




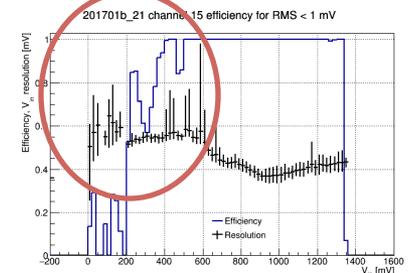
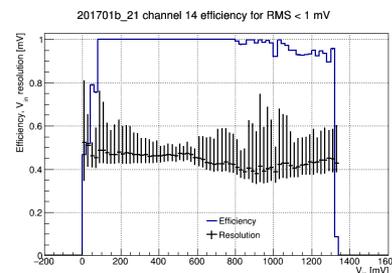
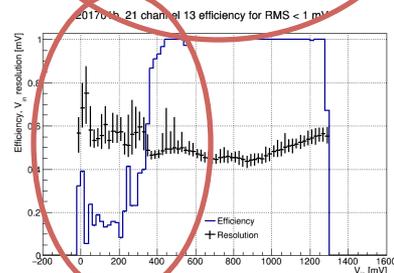
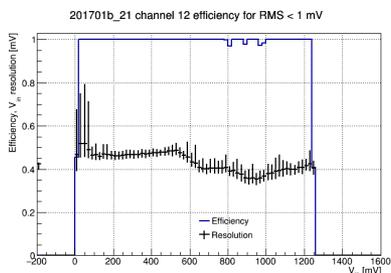
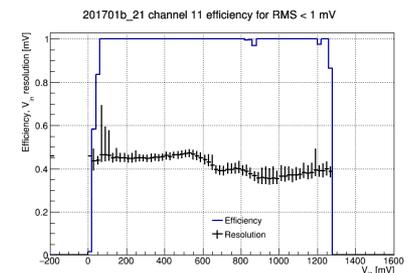
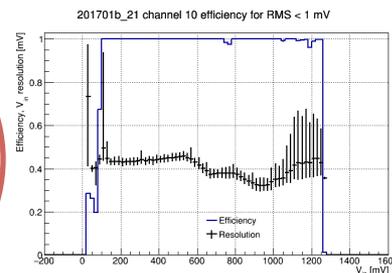
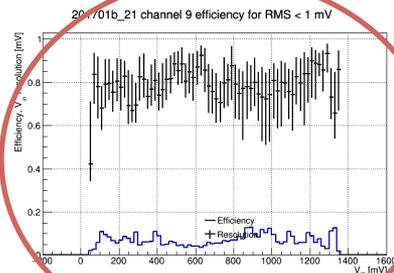
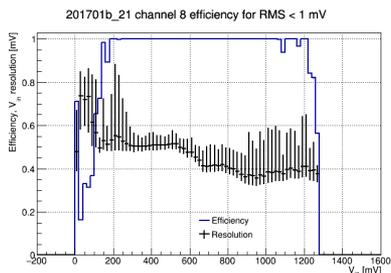
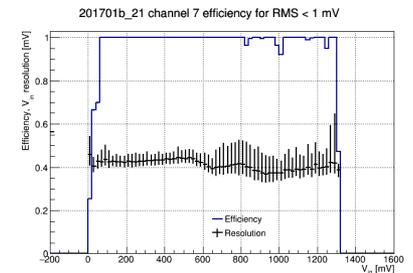
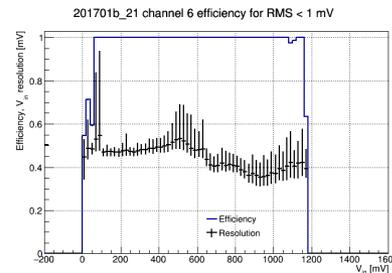
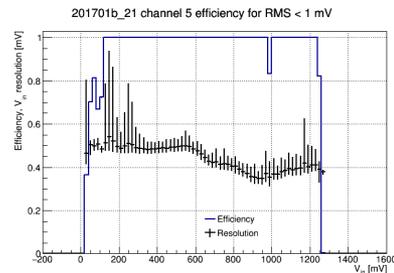
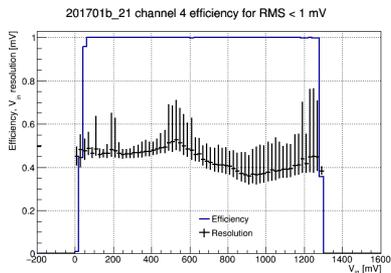
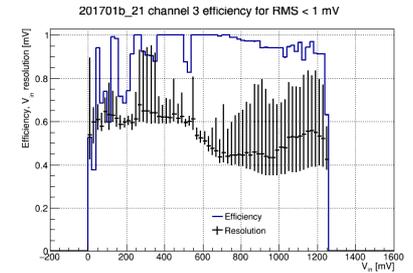
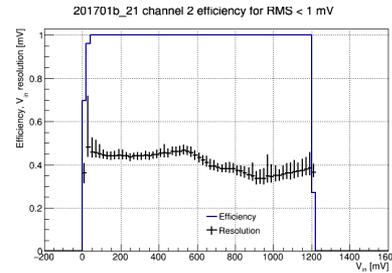
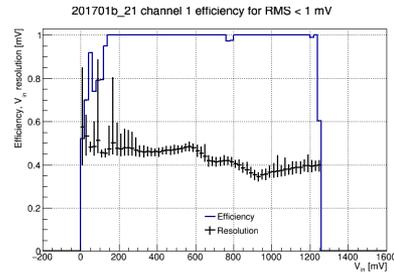
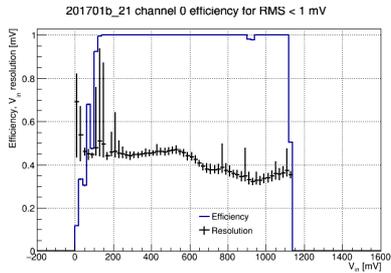
# ADC chip 17 (poor)



# ADC chip 18 (poor)



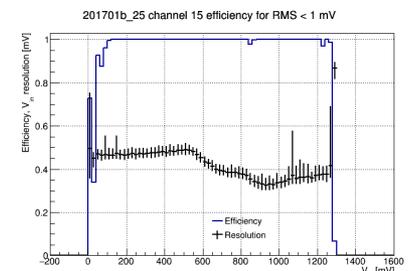
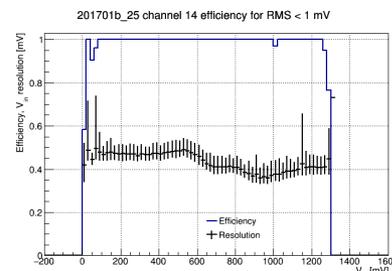
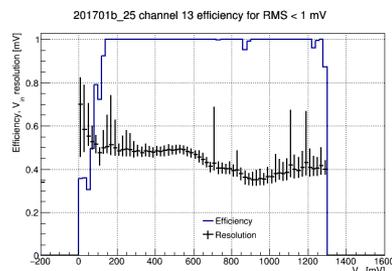
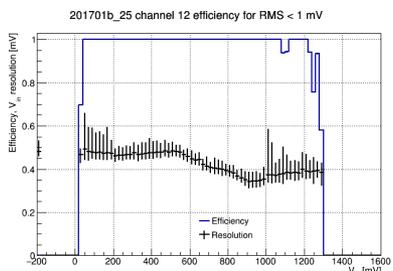
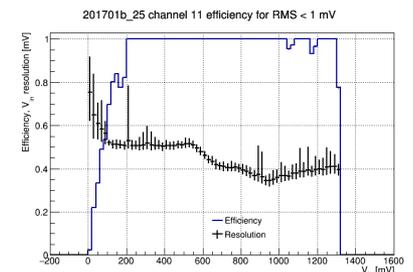
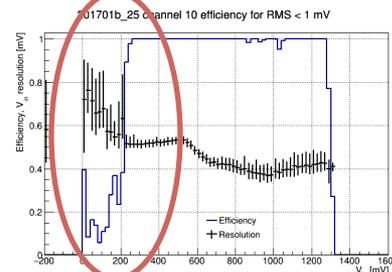
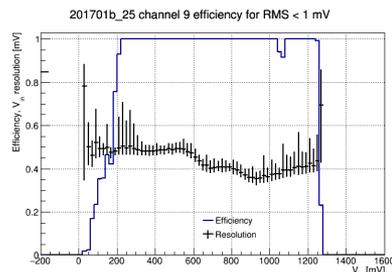
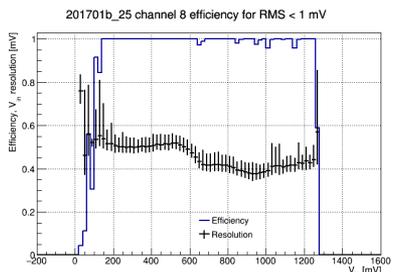
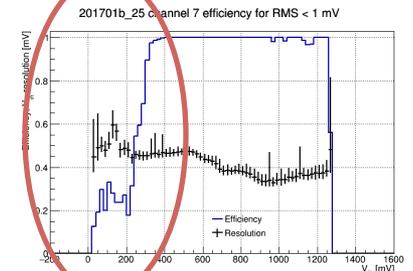
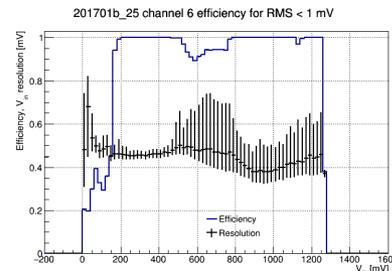
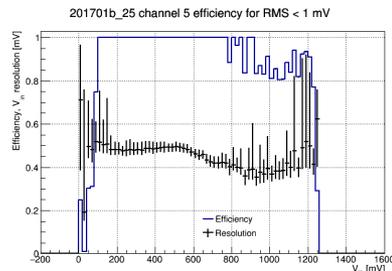
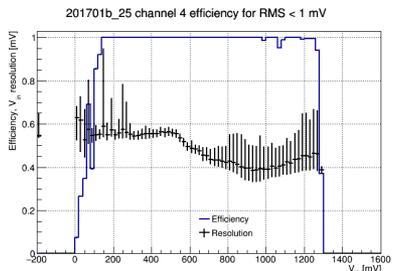
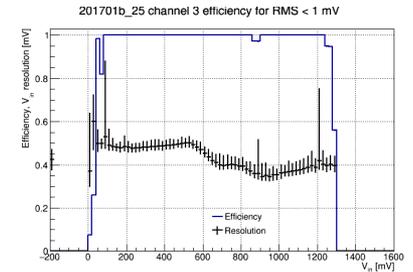
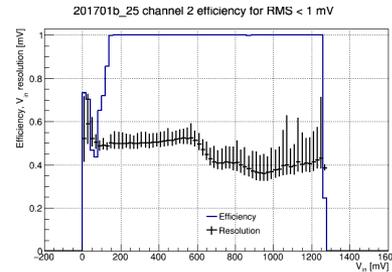
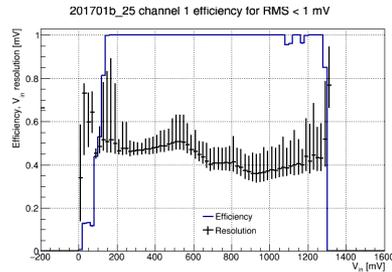
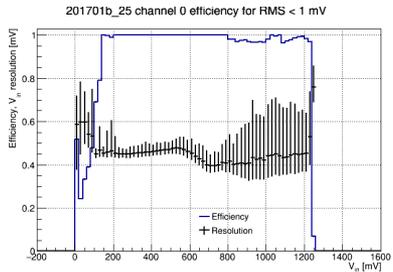
# ADC chip 21 (bad)





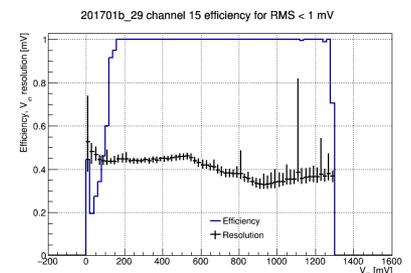
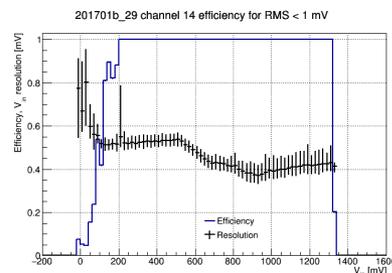
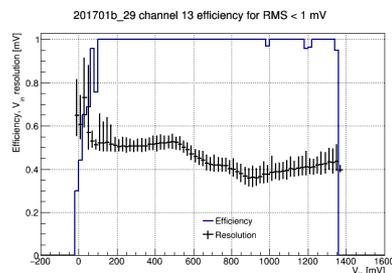
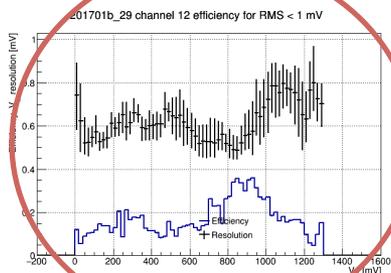
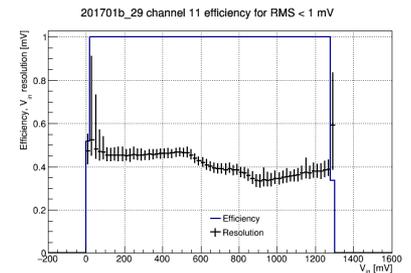
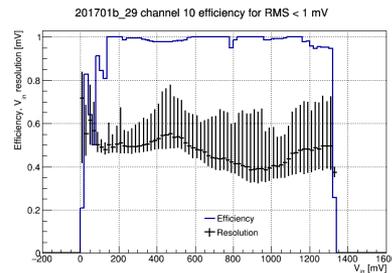
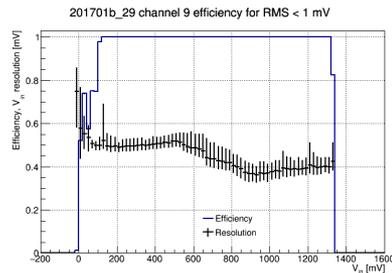
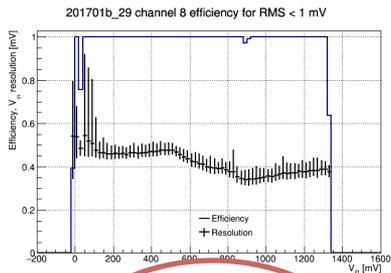
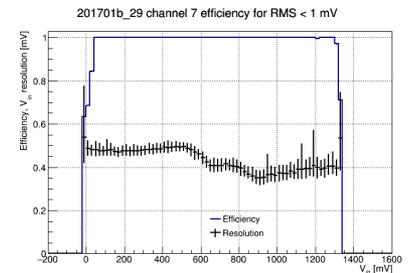
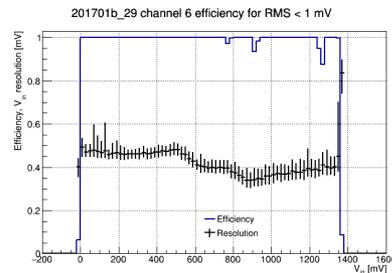
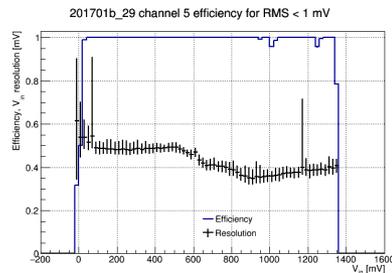
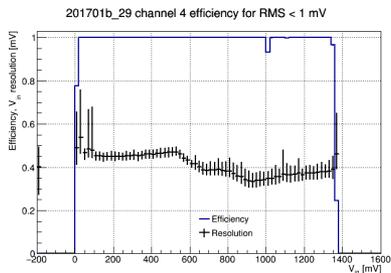
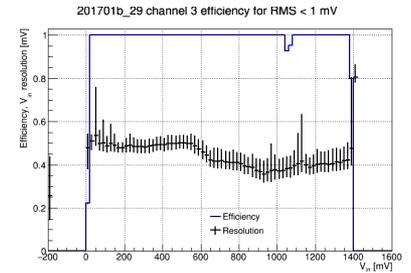
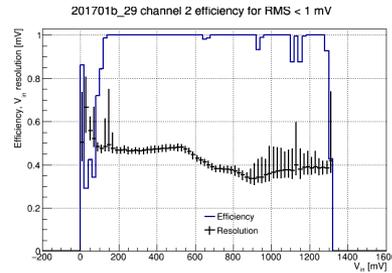
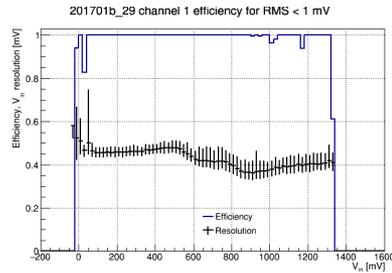
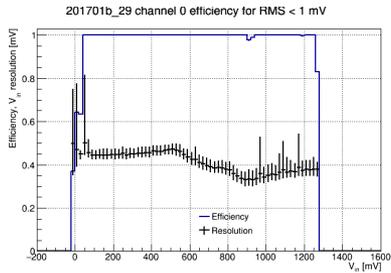


# ADC chip 25 (poor)





# ADC chip 29 (bad)











# ADC chip 35 (bad)

